WAVETEK

INSTRUCTION MANUAL

MODELS 5155A/5156A
1 MHz TO 1 GHz
FAST SWITCHING FREQUENCY SYNTHESIZERS

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WAVETEK®

WAVETEK SAN DIEGO, INC.
9045 Balboa Ave., San Diego, CA 92123
P. O. Box 85265, San Diego, CA 92138
Tel 619/279-2200 TWX 910/335-2007

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.

Models 5155A and 5156A Fast Switching Frequency Synthesizers

SECTION 1
GENERAL DESCRIPTION

- Frequency Range: 1 MHz to 1 GHz
- Frequency Resolution: 0.1 Hz
- Phase Continuous Frequency Switching
- Switching Speed: As Fast as 1 μs
- Excellent Close-in Phase Noise
- Remote Programming: BCD (standard); GPIB (option)

1.1 MODELS 5155A/5156A

Models 5155A and 5156A Programmable Frequency Synthesizers operate in the 1 MHz to 1 GHz frequency range with 0.1 Hz frequency resolution. Model 5155A has both front panel and BCD remote progamming control for complete flexibility; Model 5156A has remote BCD programming only. Remote GPIB (IEEE-488) programming is available as an option for both models.

Both instruments produce a sine output of exceptional purity and stability. The output level can be controlled in 0.1 dB steps from +3.1 to +13 dBm into 50 ohms (or in 10 mV steps for the 5155A).

The synthesizer allows for a fast frequency switch in less than 1 μs within a band up to 10 MHz wide. Larger frequency changes (greater than or equal to 10 MHz) will be settled to within the specified limits in less than 100 μs.

A Display Modifier section on the Model 5155A allows the user to modify or edit an existing frequency or amplitude value rather than require that an entire new entry be made. A flashing digit indicates which number changes. This feature may be used to manually sweep the output in frequency or amplitude.

The main RF output, whether on the front or rear panel, may be disabled through front panel control with an illuminated pushbutton. A light in the button gives an indication that the RF output is enabled.

The GPIB (General Purpose Interface Bus) interface is available as Option 006 on both units. When installed, the standard BCD interface is not sacrificed so that both interfaces may be used (though not simultaneously) — the BCD interface is usually for fast frequency programming and the GPIB for simple programming. Free format programming on the 5155A is used to enter data in any order, format or combination of scientific notation, MHz, kHz, or Hz.

1.2 SPECIFICATIONS

1.2.1 Model 5155A

FREQUENCY

Range
1 to 1000 MHz (999.999 999 9 MHz); coverage to 200 kHz, nominal, with degraded performance.

Resolution
0.1 Hz.

Control Entry
MHz, kHz, or Hz.

Switching Speed
See Remote Interface specifications.

Accuracy/Stability
Same as Reference Oscillator.

MAIN OUTPUT

Level
+3.1 dBm to +13.0 dBm into 50Ω.

Resolution
0.1 dB.

Control Entry
dBm, V, or mV.

Flatness (At +13 dBm)
<500 MHz: ±0.5 dB.
≥500 MHz: ±1 dB.

RF Output On/Off
>80 dB on/off ratio via front panel illuminated button or remote control input.

VSWR (At 1 GHz)
<1.8:1 relative to 50Ω.

Connector
Front panel Type N.

SPECTRAL PURITY

Nonharmonic
<500 MHz: −70 dBc, (−75 dBc, typical).
≥500 MHz: −64 dBc, (−69 dBc, typical).

Harmonic (At +13 dBm)
−20 dBc (−25 dBc, typical).

Sub-Harmonic
Same as Non-Harmonic specifications except 500 to 550 MHz: −56 dBc (−60 dBc, typical).

Residual Phase Noise Spectral Density
(Steady state, f <500 MHz. Reduce by 6 dB for f ≥500 MHz.)

Offset Frequency	S/N (dBc/Hz) Guar.	Typical
10 Hz	−85	−90
100 Hz	−100	−105
1 kHz	−110	−115
10 kHz	−115	−120
100 kHz	−120	−125
1 MHz	—	−130

REFERENCE OSCILLATOR

Internal
One of several optional time bases or no internal reference (Option 000) may be chosen. See Options.

External
5 or 10 MHz at 0.4 Vrms into 50Ω. Input to rear panel BNC.

Output
10 MHz at 0.4 Vrms into 50Ω. Rear panel BNC.

FRONT PANEL CONTROL

Keyboard, function and modifier buttons, and LCD readout.

Display
Frequency: 10 digit LCD readout in Hz with fixed decimal point for 0.1 Hz resolution.
Output Level: 3 digit LCD readout for 3.1 to 13.0 dBm or 0.32 to 1.00 Vrms.

Display Modifier
Control: Illuminated on/off button causes right-most digit to blink.
Digit Select: Left/right arrows (◄,►) select digit to be modified by blinking selected digit.
Modify Digit: Increments/decrements (▲,▼) selected digit. Output updated as display changes.

REMOTE BCD INTERFACE

Logic
TTL, parallel BCD, negative-true logic, double buffered.

Frequency Control
10 digits parallel; 5 remote strobes for byte serial applications.

Output Level Control
2 digits parallel; 14-pin connector; one remote strobe line; 00 to 99 for +13.0 to +3.1 dBm output.

Programming Delay (BCD Only.)
<10 MHz increment: 2 μs.
≥10 MHz increment: 0.5 μs.

Switching Transient
(To within 0.1 rad.)
<10 MHz increment (digit): 1 μs.
10 MHz increment (digit): 75 μs.
>10 MHz increment (digit): 100 μs.

Phase Continuity
Phase continuous for any frequency change using only the 6 digits below 100 kHz.

Amplitude Setting Time
50 μs.

REMOTE GPIB INTERFACE

Optional interface (006) in addition to std BCD interface. IEEE-488 1978 compatible listener/talker non-isolated, double buffered.

Interface Functions
SH1, AH1, T6, TE0, L3, LE0, SR1, RL2, PP1, DC1, DT0, C0, E1.

GPIB Timing
Frequency: 125 ms.
Amplitude: 125 ms.
RF On/Off: 30 ms.

GENERAL

Environment
Operating Temp: 0° to +40°C.
Storage Temp: −20° to +70°C.

Dimensions
48.3 cm (19 in.) wide; 13,3 cm (5.25 in.) high; 48.3 cm (19 in.) deep; includes rack ears.

Weight
18 kg (40 lb) net; 21 kg (44 lb) shipping.

Power
115/230 Vac ±10%, 47 to 63 Hz, 85 VA.

OPTIONS

One crystal option (000, 001, 002 or 004) must be selected.

000
No Internal Reference Oscillator. (External 5 or 10 MHz reference input signal required.)

001
Internal 10 MHz High Stability Crystal Reference Oscillator.
Aging Rate: $\pm 4 \times 10^{-9}$/day.
Temperature Stability: $\pm 1 \times 10^{-8}$, 0° to +40°C.

002
Internal 10 MHz TCXO Reference Oscillator
Aging Rate: $\pm 4 \times 10^{-6}$/year.
Temperature Stability: $\pm 1 \times 10^{-6}$, 0° to +40°C.

003

Rear Panel RF Output BNC. Replaces front panel type N connector.

004

Internal 10 MHz Very High Stability Crystal Reference Oscillator.

Aging Rate: $\pm 5 \times 10^{-10}$/day.

Temperature Stability: $\pm 1 \times 10^{-8}$, 0° to +40°C.

006

GPIB (IEEE-488 1978). In addition to standard BCD interface.

008

Rack Slides

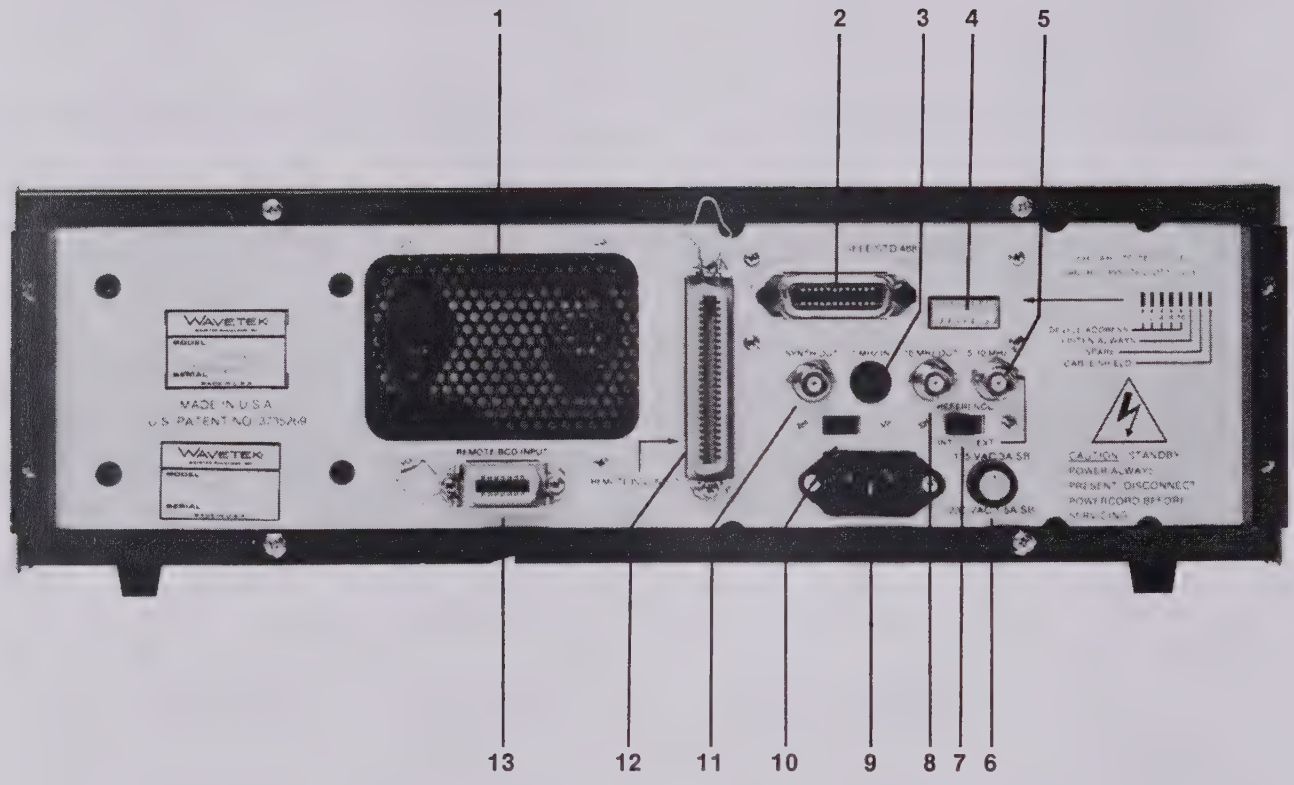
ACCESSORIES

BCD Programming Connectors

P/N 351-5001 50-pin male and 352-1401 14-pin male. Supplied with unit.

1.2.2 Model 5156A

Model 5156A is a remote control version with blank front panel.



1 Cooling
2 IEEE 488 (GPIB) Connector (Option 006)
3 1 MHz Reference Input (Option 007)
4 GPIB Address Switch (Option 006)
5 5 or 10 MHz Reference Signal Input
6 Fuse 115 Vac, 3A, Slow Blow or 230 Vac, 1.5A Slow Blow
7 Switch Selecting Source of 10 MHz Input (**6**): internal or external. External is the signal coming into 5/10 MHz IN BNC (**5**) or 1 MHz in BNC (**3**)
8 10 MHz Reference Signal Output
9 Power Cord Connector
10 115/230 Vac Input Power Adapter Switch
11 Synthesizer Output (Option 003 for 5155A)
12 BCD Frequency Control Connector
13 BCD Amplitude Control Connector

NOTE: Refer to section 2.2. for connector and switch details.

Figure 2-1. Model 5156A Rear Panel (Typical for Model 5155A)

SECTION 2
INSTALLATION & INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The synthesizers can be used as bench instruments or mounted in a standard RETMA rack since both the 5155A and the 5156A contain rack ears.

NOTE

In rack installation, the instrument must be supported at the rear of the rack since the rack ears themselves will not support the entire weight of the instrument.

Rack slides are available (Option 008) for either instrument and are designed to be installed in a 22 inch deep standard RETMA rack. Whether used on a bench or in a rack, ensure that there is no impedance to air flow at any surface of the instrument. Before rack mounting, it may be desirable to perform the initial checkout (section 2.2.6) to verify operation of all functions.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a 3A fuse.

Conversion to 230 Vac requires a change in the position of the recessed slide switch located on the rear panel. Use a small bladed screwdriver to change the position of the switch until the legend "230" for 230 Vac is visible in the recessed slot. Replace the standard 3A slow blow fuse with a 1½A slow blow fuse.

Switch Position	Input Vac	Fuse
115	103 to 126	3A
230	207 to 253	1½A

2.2.2 RF Signal Connections

NOTE

Use RG58U 50Ω or equivalent 50Ω coaxial cables equipped with proper connectors to distribute signals. The 5155A uses a type N connector for the standard front panel output and a BNC connector for the Option 003 rear panel output. Only the rear panel BNC output connector is available for the 5156A.

Front Panel:

RF Output. (5155A without Option 003). +3.1 to +13 dBm output into 50Ω; type N connector.

Rear Panel (All BNC connectors):

SYNTH OUT. (Standard on 5156A, Option 003 on 5155A). +3.1 to +13 dBm into 50Ω.

5/10 MHz IN. 0.4 Vrms into 50Ω nominal for use as the reference source. Reference must be within ±200 Hz of 10.0000 MHz.

10 MHz OUT. 0.4 Vrms into 50Ω nominal supplied from internal (or external) reference source so that other devices may be driven off of the same reference source.

2.2.3 BCD Connectors

Two connectors to allow remote control of the frequency (50-pin connector) and amplitude (14-pin connector). The panel connectors are Ansley P/N 609-50F (50-pin) and P/N 609-14F (14-pin). The mating connectors (supplied with the instrument) are Cinch P/N 57-30500 (Wavetek P/N 351.5001), and Amphenol P/N 57-30140 (Wavetek P/N 351.1401). The pin connections are given in the BCD programming section of this manual (section 3.5).

2.2.4 GPIB Connections

The GPIB I/O rear panel pin connections and signal names are given in table 2-1. The panel connector is an

Amphenol 57-20240-2 (or equivalent) and connects to a GPIB cable connector (available from Wavetek in 1 and 2 meter lengths). If the length is not specified on the purchase order, the 2 meter cable will be supplied.

2.2.5 GPIB Switch (Rear Panel)

2.2.5.1 GPIB Address

For instruments on the General Purpose Interface Bus (GPIB), ensure that the instrument GPIB address is correct and unique. The GPIB address may be changed by either the rear panel switches or the front panel GPIB Address button (5155A only). The switch position addresses are labeled 1 through 5 and shown in table 2-2 with their OFF position noted (OFF = binary "0"). To verify the address, press the GPIB Address button on the front panel of the 5155A. Upon power-up, the address is always that of the rear panel switch.

2.2.5.2 Listen Always Mode

When switch #6 is on, the synthesizer accepts data without the need to be addressed as a listener by the GPIB controller (ATN line does not have to be asserted).

Table 2-1. GPIB (IEEE-488) Data In/Out

Pin	Signal	
1	D101	True when LOW
2	D102	
3	D103	
4	D104	
5	EOI	
6	DAV	
7	NRFD	True when HIGH
8	NDAC	
9	IFC	True when LOW
10	SRQ	
11	ATN	
12	Chassis Ground (⏚)	
13	D105	True when LOW
14	D106	
15	D107	
16	D108	
17	REN	
18	GND	Signal Ground (⏚)
19	GND	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	

This is called the Listen Always mode. Any data that is sent over the GPIB will be interpreted by the synthesizer as if the instrument has been properly addressed. Unrecognizable commands will generate an SRQ by the 5155A but will be ignored by the 5156A.

NOTE

The SRQ capability will not function in the Listen Always Mode since the synthesizer is prevented from sending data (talking) to the controller.

Table 2-2. GPIB (IEEE-488) Address Codes

	ASCII		Switch Position	Hexa-decimal	
Device	Listen	Talk	1 2 3 4 5	Listen	Talk
0	(space)	@	0 0 0 0 0	20	40
1	!	A	1 0 0 0 0	21	41
2	"	B	0 1 0 0 0	22	42
3	#	C	1 1 0 0 0	23	43
4	$	D	0 0 1 0 0	24	44
5	%	E	1 0 1 0 0	25	45
6	&	F	0 1 1 0 0	26	46
7	'	G	1 1 0 0 0	27	47
8	(	H	0 0 0 1 0	28	48
9	)	I	1 0 0 1 0	29	49
10	*	J	0 1 0 1 0	2A	4A
11	+	K	1 1 0 1 0	2B	4B
12	,	L	0 0 1 1 0	2C	4C
13	—	M	1 0 1 1 0	2D	4D
14	•	N	0 1 1 1 0	2E	4E
15	/	O	1 1 1 1 0	2F	4F
16	0	P	0 0 0 0 1	30	50
17	1	Q	1 0 0 0 1	31	51
18	2	R	0 1 0 0 1	32	52
19	3	S	1 1 0 0 1	33	53
20	4	T	0 0 1 0 1	34	54
21	5	U	1 0 1 0 1	35	55
22	6	V	0 1 1 0 1	36	56
23	7	W	1 1 1 0 1	37	57
24	8	X	0 0 0 1 1	38	58
25	9	Y	1 0 0 1 1	39	59
26	:	Z	0 1 0 1 1	3A	5A
27	;	[	1 1 0 1 1	3B	5B
28	<	\	0 0 1 1 1	3C	5C
29	=	]	1 0 1 1 1	3D	5D
30	>	↑	0 1 1 1 1	3E	5E

NOTE

Address 31 is not allowed.

2.2.5.3 Compatibility Mode (5155A Only)

When switch #7 is on, the 5155A allows only those programming commands over the GPIB which would be accepted by the 5156A remote-only synthesizer. In this manner, the 5155A may be used to develop ATE programs for use on the 5156A while still providing the complete flexibility of the 5155A.

2.2.6 Initial Checkout and Operation Vertification

2.2.6.1 Local Operation (Model 5155A)

Make the equipment setup as shown in figure 2-2 and perform the steps in table 2-3 to verify Wavetek 5155A operation. Phase noise and switching speed tests, which require more elaborate setups, are briefly described in section 2.2.6.2.

A 1 GHz spectrum analyzer is recommended for nominal amplitude and frequency measurements. Accurate frequency tests require a counter whose external reference input can be connected to the synthesizer reference standard. A calibrated power meter is required for accurate amplitude measurements.

NOTE

An internal crystal reference must be installed (Option 001, 002 or 004) or an external 5/10 MHz input signal must be supplied to the 5155A in order for the instrument and display to function properly. The synthesizer is provided with standby power for the internal oscillator so that crystal aging is maintained and initial turn on warmup performance can be avoided during normal synthesizer power down. Crystal accuracy is factory tested but can be checked regularly after 24 hours of initial turn on to verify the crystal aging rate. The crystal should be compared or measured with a calibrated reference standard. A frequency adustment is provided on the oscillator to rèset the 10 MHz crystal frequency as necessary.

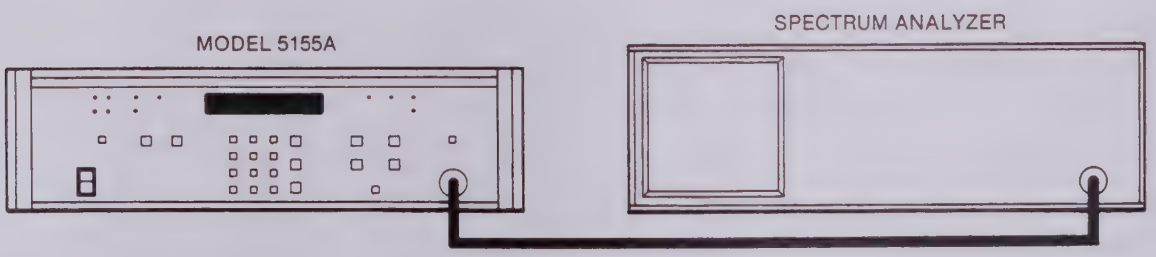


Figure 2-2. Initial Checkout

Table 2-3. Initial Checkout – Local Operation

Step	Test	Setup	Program	Desired Results
1	Wake-up Status		Power: On	All LEDs flash for 2 sec. Display: 250,000,000.0 (Hz)
2	GPIB Address		Press: GPIB Address	Display: Rear-panel-set GPIB address.
3			Press: GPIB Address 03	Display:03
4			Press: 28	Display: 28

Table 2-3. Initial Checkout-Local Operation (Continued)

Step	Test	Setup	Program	Desired Results
5	Frequency Coverage	RF Spectrum Analyzer or Frequency Counter (Connect counter reference to synthesizer 10 MHz reference)	Press: Freq 1 MHz	Display: 1,000,000.0 (Hz) Analyzer: Signal at 1 MHz
6			Press: 999 MHz	Display: 999,000,000.0 (Hz) Analyzer: Signal at 999 MHz
7			Press: 100 MHz	Display: 100,000,000.0 (Hz) Analyzer: Signal at 100 MHz
8		See figure 2-2. RF Spectrum Analyzer Center Freq: 500 MHz Freq Span: 100 MHz/div Res BW: 1 MHz Input Atten: 30 dB Ref Level: 20 dB; 10 dB/div	Press: (Display Modifier) On	Display: Rightmost digit flashes Button LED: Lit
9			Press: ► once	Display: Leftmost digit flashes.
10			Press: ▲once	Display: 200,000,000.0 (Hz) Analyzer: 200 MHz signal
11			Press: ▲ seven times	Display: Changes in 100 MHz digit increments to 900 MHz. Analyzer: Signal moves in 100 MHz steps.
12			Press: (Display Modifier) On	Button LED: Extinguished
13	Error Detection		Press: Freq 125 MHz	Display: 125,000,000.0 (Hz)
14			Press: 1000 MHz	Display: 1000 flashing
15			Press: Clear	Display: 125,000,000.0 (Hz)
16	Amplitude Flatness	Spectrum Analyzer or RF Power Meter	Repeat steps 5 – 11	Measure full scale amplitude and record results in checkout record.
17	Attenuator	Spectrum Analyzer or RF Power Meter	Press: Ampl	Display: 13.0 (dBm) Analyzer: 13 dBm
18			Press Ampl 3.1 dBm	Display: 3.1 (dBm) Analyzer: Signal level decreases 10 dB
19			Press: Volt	Display: .32 (Volt)
20			Press: 13.0 dBm	Display: 13.0 dBm
21	Nonharmonic Spurious Check	RF Spectrum Analyzer Center Freq: 100 MHz Freq Span: 2 MHz/Div RES BW: 100 kHz Input Atten: 30 dB REF Level: 27 dB; 10 dB/div	Press: Freq 100 MHz	Display: 100 MHz Analyzer: 100 MHz
22			Press: (Display Modifier) On Press: ► 4 times	Button LED: Lit 100 kHz digit flashing

Table 2-3. Initial Checkout-Local Operation (Continued)

Step	Test	Setup	Program	Desired Results
23	Nonharmonic Spurious Check	RF Spectrum Analyzer Center Freq: 100 MHz Freq Span: 2 MHz/div RES BW: 100 kHz Input Atten: 30 dB REF Level: 27 dB; 10 dB/div	Press: ▼ Hold until frequency reaches 90 MHz	Observe and enter data as needed on checkout record.
24			Press: ▲ Hold until frequency reaches 110 MHz	
25			Repeat steps 5 – 11	
26	Subharmonic Spurious Check	Spectrum Analyzer	Press: ▼ until display reads 500 MHz	Observe spurious signals at 250 and 750 MHz and enter data as needed on checkout record.
27	Harmonic Spurious Check		Repeat steps 5 – 11	Observe and enter data as needed on checkout record.

2.2.6.2 Additional Performance Verification Tests

Phase Noise Measurement

Phase noise measurement is accomplished by adjusting two double balanced mixer inputs to the same frequency. These two inputs are the unit under test and a reference tone with phase noise characteristics equal to or better than the unit under test. The reference source is phase locked to the unit under test. The mixer output is low passed to remove the sum frequency. A dc level is set to zero by adjusting the inputs to be 90 degrees out of phase. The resulting noise on the mixer output is spectrum analyzed to display the frequency distribution of the signal. For more information about this test, see Wavetek San Diego Application Note 55.

Switching Speed Measurement

The test setup for switching speed is similar to phase noise except that an oscilloscope is used to monitor the results instead of a spectrum analyzer. One input to the mixer is a reference tone. The second is the unit under test hopping back and forth from one frequency to another. The mixer is used as a phase detector by adjusting the reference tone to be in quadrature with one of the frequencies of the unit under test. Delay and settling times are measured on the oscilloscope from the programming pulse. For more information, see Wavetek San Diego Application Note 54.

Table 2-3. Initial Checkout — Local Operation (Continued)
5155A Checkout Record S/N _____

Paragraph or Reference	Desired Results	Accept
2.2.1	Correct Fuse Installed Correct Voltage Selected	_____ _____
2.2.6.1	Reference Source Selected	_____
5	Frequency Coverage (11 frequencies tested)	_____
13	Error Detection	_____
16	Amplitude Flatness 1 MHz _____ 600 MHz _____ 100 MHz _____ 700 MHz _____ 200 MHz _____ 800 MHz _____ 300 MHz _____ 900 MHz _____ 400 MHz _____ 999 MHz _____ 500 MHz _____	_____
17	Attenuator Display	_____
18	Attenuation Range, 10 dB nominal	_____
23 – 25	Nonharmonic Spurious Check 1 MHz _____ 600 MHz _____ 100 MHz _____ 700 MHz _____ 200 MHz _____ 800 MHz _____ 300 MHz _____ 900 MHz _____ 400 MHz _____ 999 MHz _____ 500 MHz _____	_____
26	Subharmonic Spurious Check 500 MHz _____	_____
27	Harmonic Spurious Check 1 MHz _____ 600 MHz _____ 100 MHz _____ 700 MHz _____ 200 MHz _____ 800 MHz _____ 300 MHz _____ 900 MHz _____ 400 MHz _____ 999 MHz _____ 500 MHz _____	_____

Table 2-3. Initial Checkout — Local Operation (Continued)
5155A Checkout Record

S/N _____

Paragraph or Reference	Desired Results	Accept
2.2.6.2	Phase Noise Test Offset from carrier 10 Hz _____ 100 Hz _____ 1 kHz _____ 10 kHz _____ 100 kHz _____	_____
	Switching Speed Digit 10 kHz _____ 100 KHz _____ 1 MHz _____ 10 MHz _____ 100 MHz _____	_____

2.2.6.2 Remote BCD Operation

To verify BCD operation, certain pins must be grounded (to give BCD input) and a TTL level pulse furnished to other pins (latch strobes to capture the BCD input). A minimum apparatus to accomplish this is implied in figure 2-3.

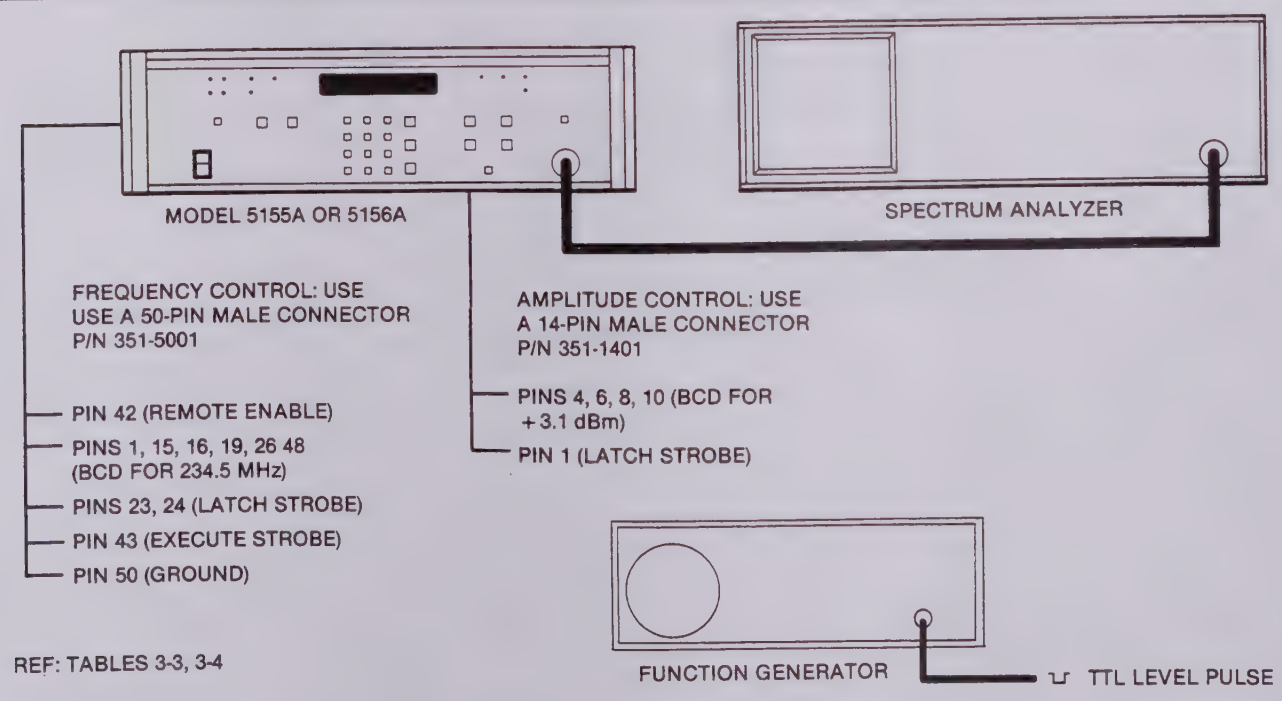


Figure 2-3. BCD Test Setup

Table 2-4. Initial Checkout – Remote BCD Operation

Step	Test	Setup	Action	Desired Results
1	Wake-up Status	See figure 2-3.		5155A: All LED's flash for 2 sec. 5156A: BCD LED On.
2	Remote (5155A only)	On 50-pin connector: Ground "Remote Enable"		BCD Active LED: On Front Panel Active LED: Off Front Panel Lockout LED: On
3	Frequency	On 50-pin connector: Ground "BCD for 234.5 MHz" pins	Apply a TTL pulse to 50-pin connector "Latch Strobe"	No change
4			Apply a TTL pulse to 50-pin connector "Execute Strobe"	5155A: Display of 234,500,000.0 (Hz) Analyzer: 234.5 MHz signal
5	Initial Amplitude (5155A only)	Remove ground from "Remote Enable"		BCD Active LED: Off Front Panel Active LED: On Front Panel Lockout LED: Off
6			Press Ampl	Display: 13.0 (dBm) Analyzer: 13 dBm
7	Remote	Ground "Remote Enable"		BCD Active LED: On Front Panel Active LED: Off Front Panel Lockout LEd: On
8	Amplitude	On 14-pin connector, ground "BCD for +3.1 dBm" pins	Apply a TTL pulse to 14-pin connector "Latch Strobe"	No change
9			Apply a TTL pulse to 50-pin connector "Execute"	5155A: 3.1 (dBm) Analyzer: Signal reduced 10 dB

2.2.6.3 GPIB (Option 006) Operation (Model 5155A)

Connect the equipment as shown in figure 2-4 and perform the steps in table 2-5 to verify the GPIB operation of the Model 5155A. The Wavetek 6000 Instrumentation Controller is used to check out the synthesizer (device address 07) in table 2-5. If another controller is used, please refer to the operator's manual of the controller for the proper commands needed to send and receive data over the GPIB. For more information on GPIB operation, refer to section 3.7 of this manual.

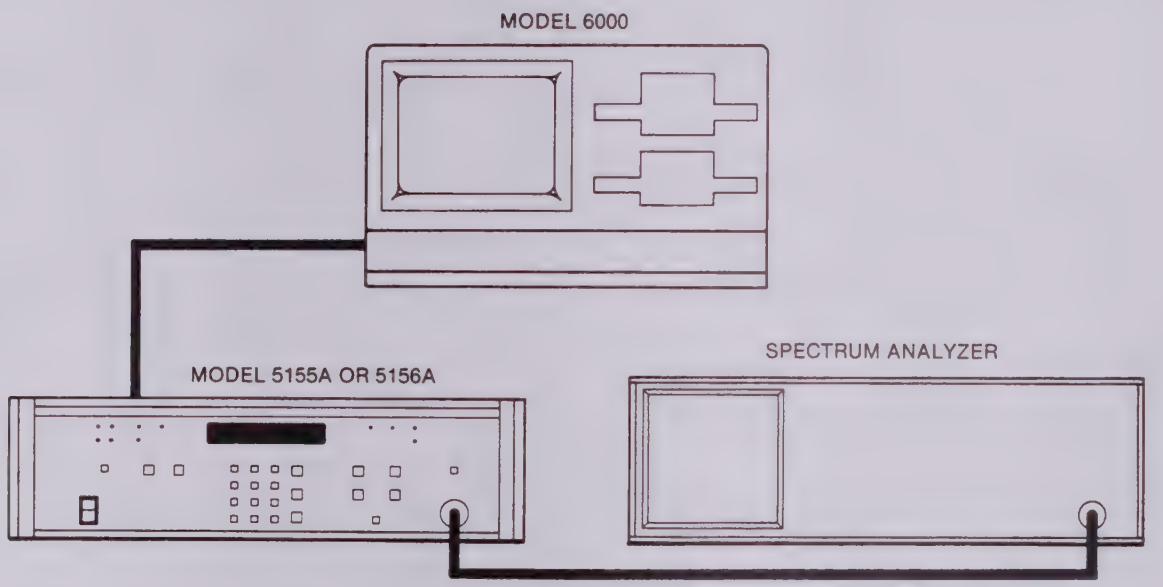


Figure 2-4. GPIB (IEEE-488) Equipment Setup

Table 2-5. Initial Checkout — Model 5155A GPIB (IEEE-488) Operation

Step	Test	6000 Command	5155A Program	Desired Results
1	Wake-up Status		Power: On	All LEDs flash for 2 sec. Display: 250,000,000.0 (Hz). Front Panel Active LED: On.
2	Enable Remote	REN @707		GPIB Active LED: On.
3	Enter Listen (Ref: section 3.7.5)	WRITE @707: "FREQ 125.987M"		Display: 125,987,000.0 (Hz). GPIB Active LED: On. GPIB Listen LED: On. Front Panel Active LED: On. Analyzer: Signal at 250 MHz.

Table 2-5. Initial Checkout – Model 5155A GPIB Operation (Continued)

Step	Test	6000 Command	5155A Program	Desired Results
4	Frequency Change	WRITE @707: "EXECUTE"		Display: No change. Analyzer: Signal at 125.987 MHz.
5	Amplitude Change	Press Ampl.		Display: 13.0 (dBm).
6		WRITE @707: "AMP 8DB @ E"		Display: 8.0 dBm. Analyzer: Signal reduced by 5 dB.
7	RF Off (Ref: section 3.4.1.3)	WRITE @707: "RF OFF"		RF Output button LED: Off. Analyzer: No signal.
8	RF On	WRITE @707: "RF ON"		RF Output button LED: On. Analyzer: 125.987 MHz signal at 8 dBm.
9	Display Modifier Mode (Ref: section 3.4.1.1)	WRITE @707: "MOD ON"		Display: Rightmost digit begins blinking.
10		WRITE @707: "MOD LEFT"		Display: "8" begins blinking.
11		WRITE @707: "MOD UP"		Display: "8" becomes a blinking "9".
12		WRITE @707: "MOD OFF"		Display: "9" stops blinking.
13	Reset Instrument	DCL @707		Display: 250,000,000.0 (Hz). GPIB Active LED: On. GPIB Listen LED: Off.
14	Enter Talk (Ref: section 3.7.6)	DIM D$*32		Dimension string array.
15		WRITE @707: "STATE"		GPIB Active LED: On. GPIB Listen LED: On.
16		READ @707: D$		GPIB Talk LED: On.
17		WRITE @0: D$		6000 Display: F = 250000000.0 Hz, A = 13.0 DB, RF ON

Table 2-5. Initial Checkout – Model 5155A GPIB Operation (Continued)

Step	Test	6000 Command	5155A Program	Desired Results
18	Local Lockout	LLO @7		Front Panel Active LED: Off. Front Panel Locked Out LED: On.
19	Local	LCL @7		Front Panel Active LED: On. Front Panel Locked Out LED: Off.
20	SRQ (Ref: section 3.7.6.2)	REN @707		GPIB Active LED: On.
21		WRITE @707: "F125MHZ"		GPIB Listen LED: On. SRQ LED: On.
22	Clear SRQ (Ref: table 3-5)	STATUS @707: S		.SRQ LED: Off.
23		WRITE @0: S		6000 Display: 65 (Indicates unrecognizable command. Requires space after 'F'.)
24	Compatibility Mode (Ref: section 3.7.2.1)	Depress rear switch #7		Nothing visible on synthesizer.
25		WRITE @707: "F 123 M @ E"		Display: 123,000,000.0 (Hz) Analyzer: 123 MHz signal.
26		WRITE @707: "RF OFF"		SRQ LED: On.
27		STATUS @707: S		SRQ LED: Off.
28		WRITE @0: S		6000 Display: 80 (Indicates statement not allowed in compatibility mode.)

2.2.6.4 GPIB (Option 006) Operation (Model 5156A)

Connect the equipment as shown in figure 2-4 and perform the steps in table 2-6 to verify the GPIB operation of Model 5156A. The Wavetek 6000 Instrumentation Controller is used to check out the synthesizer (device address 07) in table 2-6. If another controller is used, please refer to the operator's manual of the controller for the proper commands needed to send and receive data over the GPIB. For more information on the GPIB operation of the Model 5156A, refer to section 3.7 and Appendix C of this manual.

Table 2-6. Initial Checkout — Model 5156 GPIB (IEEE-488) Operation

Step	Test	6000 Command	5156A Settings	Desired Results
1	Wake-up State	Power: On		BCD LED: On
2	Enable Remote	REN @707		BCD LED: Off GPIB LED: On
3	Frequency Change	WRITE @707: "F 125 MH"		Analyzer: 125 MHz signal at +13 dBm
4	Amplitude Change	WRITE @707: "A 3.1D"		Analyzer: Signal amplitude reduced 10 dB
5	Listen Always		GPIB Address Switch #6: On	Nothing on 5156A
6		Power: Off then On		Analyzer: No signal
7		WRITE @730: "F 350 M"		Analyzer: 350 MHz signal at +13 dBm

SECTION 3
OPERATION

3.1 INTRODUCTION TO OPERATION

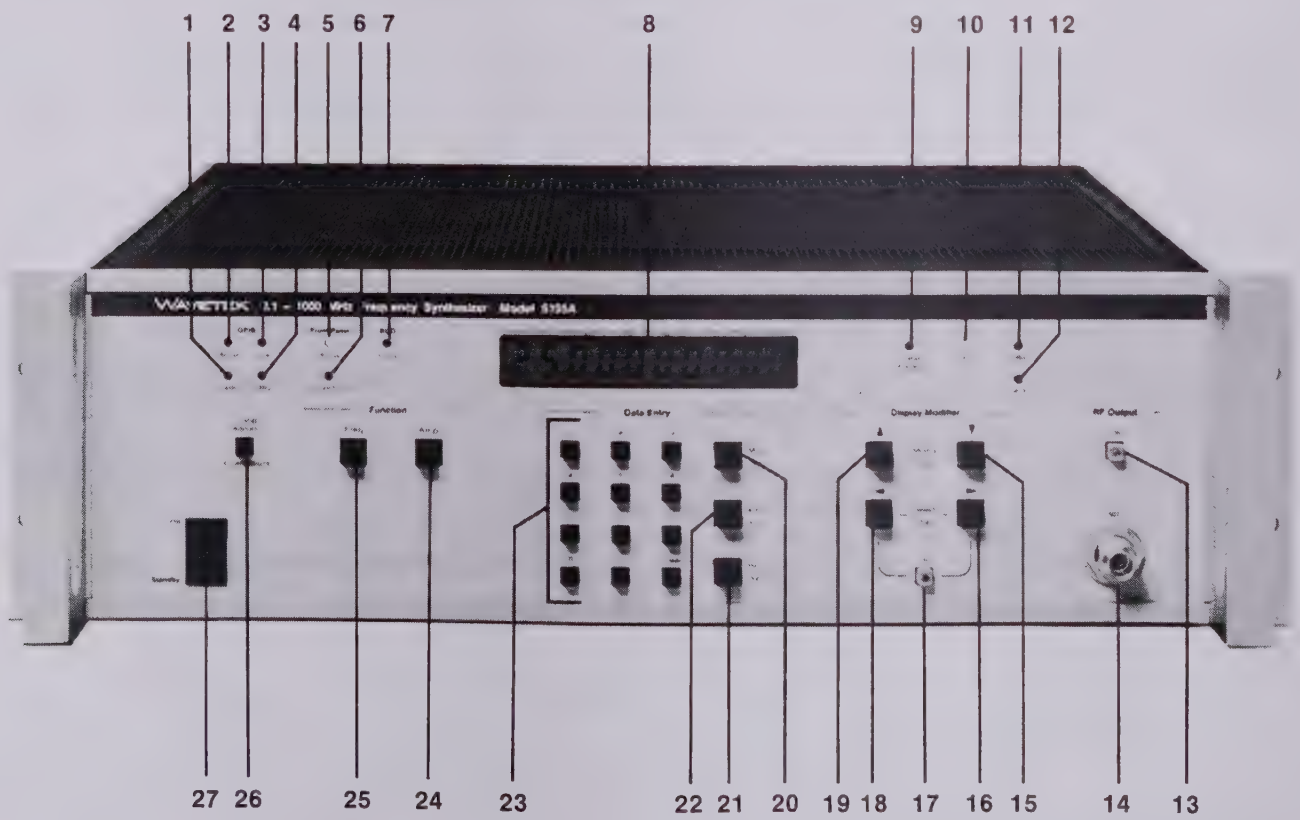
In this section all features of the front panel are explored to enable the user to become familiar with the operation of the instrument. In addition, remote control via the standard BCD interface and the optional GPIB interface for both the 5155A and the 5156A are discussed. Users of the 5155A who plan to control the instrument remotely should read both the local and remote sections.

A spectrum analyzer is the recommended instrument for verifying the basic operation of the 5155A. However, an oscilloscope may be used to determine that an output is present and that changes in the front panel settings do, in fact, result in a change in the output frequency and level.

3.2 FRONT PANEL CONTROLS AND CONNECTORS

3.2.1 Model 5155A

The front panel contains the power switch, keyboard, display, and (unless Option 003, rear panel connector, has been specified) the type N output signal connection jack. Figure 3-1 shows the location of all front panel controls and connectors. Table 3-1, which is keyed to the numeric identifiers in figure 3-1, briefly lists the purpose of each control or connector for quick reference. Further information on the controls is contained in section 3.4, Local Operation.



NOTE: Refer to table 3-1 for feature details.

Figure 3-1. Model 5155A Controls and Connectors

Table 3-1. Controls and Connectors

Key Ref No.	Control or Connector	Description
1	GPIB Listen LED	Indicates when instrument has been addressed as a listener on GPIB. It does not indicate that synthesizer is under remote control.
2	GPIB Active LED	Indicates that remote enable (REN) on GPIB is true and that the GPIB interface is the active remote interface. Will not illuminate if BCD remote enable line (see section 3.5) is low true.
3	GPIB Talk LED	Indicates when synthesizer has been addressed to send data to a controller by GPIB.
4	GPIB SRQ LED	Indicates that the synthesizer is requesting the attention of the controller by setting bit No. 6 in the serial poll register. Alerts user that error in programming command exists. See section 3.7.6.2.
5	Front Panel Active LED	Indicates that front panel controls are still active.
6	Front Panel Locked Out LED	Indicates that either BCD or GPIB interface is controlling the synthesizer functions. An active BCD interface automatically causes this LED to illuminate. While under GPIB control, the Local Lockout command must be issued.
7	BCD Active LED	Indicates that remote enable line (pin 42) of the BCD interface is true (low) and that the BCD interface is the active remote interface. Takes priority over GPIB interface if both are connected (see section 3.5).
8	(Display)	Ten digit numeric LCD readout. Used to display frequency, amplitude, and GPIB Address information as selected by buttons **25**, **24** and **26** respectively.
9	GPIB Address LED	LED indicates that display (**8**) is showing 2 digit GPIB Address.
10	Hz LED	LED indicates that display (**8**) is showing synthesizer frequency value in Hz with 0.1 Hz resolution.
11	dBm LED	LED indicates that display (**8**) is showing synthesizer amplitude level in dBm. Range of values is +3.1 to +13.0 dBm.
12	Volt LED	LED indicates that display (**8**) is showing synthesizer amplitude level in volts. Range of values is 0.32 to 1.00V.
13	RF Output On	Illuminated button indicates when main output is turned on. LED will extinguish when output is disabled. A greater than 80 dB on/off ratio is possible.
14	50Ω (Output)	The main output, a Type N connector. (Connector on back panel if rear output Option 003 is ordered.) **13** sets output at on or off with 50Ω impedance.
15,19	Modify Digit ▼,▲	Increments (▲) or decrements (▼) flashing digit in display (**8**). Changes values at 1 number/s rate. When button is held in for more than 3 seconds, the display changes at 20 numbers/s rate.

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
16, 18	Select Digit ◄,►	Moves flashing digit in display (**8**) to left (◄) or right (►) in single steps. Flashing digit can be wrapped around display to move from one side to the other quickly.
17	On	Activates Display Modify mode on display (**8**) by causing rightmost digit in display to begin flashing. LED in button illuminates. Editing mode may be terminated by pressing this button a second time or pressing either Freq (**25**) or Ampl (**24**).
18	Select Digit ◄	(See **16**).
19	Modify Digit ▲	(See **15**).
20	MHz/dBm	Terminator used to complete data entry for both frequency and amplitude. Causes either Hz or dBm LED to illuminate (**10** and **11**) depending on whether Freq or Ampl button was first pressed. Frequency data is in MHz while amplitude data is in dBm when this button is used to complete the entry.
21	Hz/mV	Terminator used to complete data entry for both frequency and amplitude. Causes either Hz or Volt LED to illuminate (**10** and **12**) depending on whether Freq or Ampl button was first pressed. Frequency data is in Hz while amplitude data is in mV when this button is used to complete the entry.
22	kHz/Volt	Terminator used to complete data entry for both frequency and amplitude. Causes either Hz or Volt LED to illuminate (**10** and **12**) depending on whether Freq or Ampl button was first pressed. Frequency data is in kHz while amplitude data is in volts when this button is used to complete the entry.
23	(Numeric Keyboard)	Data entry buttons used to change frequency, amplitude, or GPIB address. Data terminators (**20**, **21** and **22**) used to complete data entry.
24	Ampl	Causes display to readout synthesizer amplitude level in either dBm (+3.1 to +13.0) or volts (0.32 to 1.00), which is controlled by **20**, **21** and **22**.
25	Freq	Causes display to readout synthesizer frequency setting (100 kHz to 999.999 999 9 MHz) in Hz.
26	GPIB Address	Displays the GPIB decimal address and enables front panel setting of address (00 through 30).
27	On/Standby	Turns synthesizer to On or to Standby. Standby position maintains power to crystal and other circuitry where warm-up time would be greatly increased if power is removed.

3.2.2 Model 5156A

This remote-only version of the 5155A does not contain any front panel controls or connectors. The power switch and indicator LEDs are located on the front panel and are shown in figure 3-2. A brief description of each of these items is listed in table 3-2 and is keyed to the numeric identifiers in figure 3-2.

3.3 POWER-UP

When ac power is applied to the instrument, a warmup period is required if an internal reference crystal oscillator, either Option 001 (High Stability Crystal Reference), Option 004 (Very High Stability Crystal) or Option 002 (Temperature Compensated Crystal Oscillator) has been specified.

If either High or Very High Stability Crystal (Option 001 or 004) is installed, a period of 60 minutes after power is applied is required for the output frequency to be within $\pm 1 \times 10^{-7}$ of the frequency setting. No warm-up time is necessary for the Temperature Compensated Crystal (Option 002), but it is good practice to allow some time (for example, 20 minutes) for the unit to warm up.

3.3.1 Model 5155A

When ac power is applied to the instrument, it wakes up in a default state. During the first second, the microprocessor does some internal memory diagnostics as evidenced by the flashing LEDs on the front panel. Immediately following this power-up, the LCD display shows the default frequency:

250,000,000.0

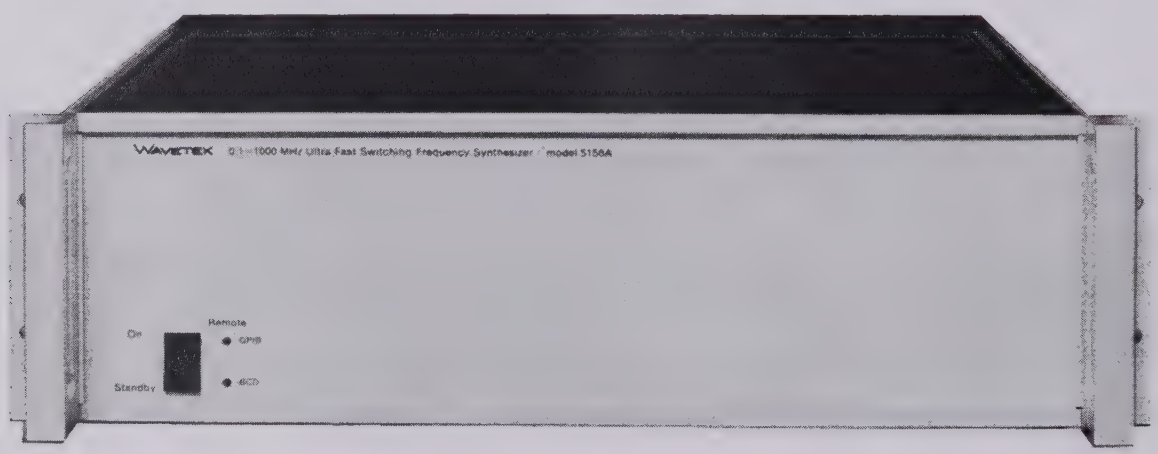
This signifies that 250 MHz has been set up in the 5155A.

NOTE

If no internal crystal reference is supplied (Options 001, 002 or 004), the power up diagnostics and display will fail unless the external reference signal, Option 000, is connected.

The various default parameters are:

Parameter	Condition
Frequency	250 MHz
Amplitude	+13.0 dBm
GPIB Address	(As set on rear panel)
Display Modifier	Off
RF Output	On
Readout	Hz



NOTE: Refer to table 3-2 for feature details.

Figure 3-2. Model 5156A Controls

Table 3-2. Model 5156A Controls

Key Ref No.	Control or Connector	Description
1	On/Standby	Turns synthesizer to On or to Standby. Standby position maintains power to crystal and other circuitry where warm-up time would be greatly increased if power is removed.
2	BCD LED	Indicates that remote enable line (pin 42) of the BCD interface is true (low) and that the BCD interface is the active remote interface. Takes priority over GPIB interface if both are connected (see section 3.5).
3	GPIB LED	Indicates that remote enable (REN) on GPIB is true and that the GPIB interface is the active remote interface. Will not illuminate if BCD remote enable line (see section 3.5) is low true.

3.3.2 Model 5156A

The 5156A has no front panel and no microprocessor to control buttons and displays. When ac power is applied to the 5156A, the BCD LED will illuminate if there are no cables connected to the rear panel programming connectors. If a GPIB controller is connected to the instrument and the remote line (REN) is true (low), the GPIB LED will illuminate and the BCD LED will be extinguished. Refer to section 3.5 for a discussion on interface priority.

The 5156A does not generate an output signal until a frequency is programmed into the synthesizer. The amplitude level is pre-programmed to maximum output level (+13.0 dBm) so data does not have to be supplied to the separate 14-pin programming connector. Refer to section 3.6 and 3.7 for more details on remote programming.

NOTE

If the 5156A does not receive data followed by an Execute strobe, there will be no output signal.

3.4 LOCAL OPERATION

Local operation is via the pushbuttons on the front panel of the 5155A. No local operation is possible with the Model 5156A. The front panel pushbuttons fall into four general categories:

1. Action buttons, which cause an immediate action on the output of the synthesizer when pressed.
2. Parameter buttons, which display the current value of a parameter (i.e., Frequency), but do not cause any action until some additional action is taken.
3. Numeric buttons, which are used for entry of numeric data. These buttons are "•" and 0 through 9.
4. Terminator buttons, which are used to complete a numeric entry and then cause an action. They do not cause an action by themselves.

Appendix B, 5155A GPIB Programming Command Summary, lists the ASCII characters associated with each button and also lists ASCII commands for functions which have no corresponding front panel pushbutton. Remote operation of the 5155A is covered in sections 3.6 and 3.7 of this manual.

3.4.1 Action Keys

The Display Modifier buttons, Clear and RF Output cause an immediate action and do not require the entry of a numeric value.

3.4.1.1 Display Modifier Buttons

The five buttons contained in the Display Modifier section — ▲, ▼, ◄, ►, and On are used to modify a parameter value and cause an immediate execution of the new value. The Modify Digit buttons (▲,▼) are used to increment and decrement a parameter value. With the button continuously held down, values change at a 1 second rate for the first 3 seconds, then change each 50 ms.

NOTE

Values cannot be changed past their allowable limits. The display will stop at either limit and the entire display will flash to indicate that an unacceptable number entry was attempted. The limit value will be the number used at the output.

The Select Digit buttons (◄,►) move the blinking digit to the desired position in the display so that the Modify Digit buttons can be used to change the values. The Select Digit buttons can only be moved one step at a time.

The GPIB Address parameter cannot be modified. Data must be entered as desired.

The On button must be pressed first before any of the other buttons in this section will operate. The LED in the button will illuminate to indicate that the Display Modify mode has been activated and the rightmost digit on the display will begin to blink. Data may now be modified with the Modify Digit buttons and the Select Digit buttons.

HINT

When the Display Modify mode has been activated, data may be entered into any digit directly. Thus, if the blinking digit displays the number "2" and the number "7" is desired, pressing the "7" in the Data Entry keyboard will cause the digit to change to a "7" immediately.

3.4.1.2 Clear

The Clear button in the Data Entry keyboard can be used to reset the display back to the last valid numeric entry for the selected parameter. It may be used in the middle of entering data or if an invalid number was entered. Pressing the parameter function buttons (GPIB Address, Freq, and Ampl) will have the same effect.

NOTE

The Clear button will not completely zero out the display. It will only clear the display back to the last valid entry.

3.4.1.3 RF Output

This illuminated button enables or disables the output signal circuitry. The instrument powers up with the RF Output enabled and, therefore, the LED in the button is lit. When the RF output is disabled, the signal is attenuated more than 80 dB.

NOTE

The RF Output button is not intended for use in pulse modulation applications. It is made availble simply to provide a quick means of turning off the output during testing.

3.4.2 Parameter Buttons

The parameter buttons (GPIB Address, Freq, or Ampl) allow the current parameter value to be displayed, then changed with the numeric Data Entry or the Display Modifier buttons.

Either the Freq or Ampl button may be used to terminate the Display Modify mode and de-activate the blinking digit.

3.4.2.1 Frequency (Freq)

The Freq button selects the Hz indicator and displays the current frequency setting. Valid frequency values are 1 to 999.9999999 MHz. A terminator button (MHz, kHz or Hz) must be pressed for the output to be updated.

3.4.2.2 Amplitude (Ampl)

The Ampl button causes the readout to display the current amplitude level setting. Valid amplitude values are +3.1 to +13.0 dBm or 0.32 to 1.00 volt. A terminator button (dBm, Volt or mV) must be pressed for correct amplitude units and for the output to be updated.

3.4.2.3 GPIB Address

The GPIB Address button displays the current device address for the synthesizer. Upon power-up, the rear panel GPIB dip switch setting is read into memory and displayed when the front panel GPIB address button is pressed. If the value is changed with the Data Entry keyboard buttons, the display will always reflect the current address. No terminator button is needed to complete the entry, but 2 digits must always be used (i.e., "06"). The rear panel setting can only be restored by turning power off and on again.

NOTE

*The Display Modifier buttons **cannot** be used to change the GPIB Address. Data must be entered through the Data Entry keyboard.*

3.4.3 Numeric Buttons

The Data Entry numeric buttons 0 through 9, and "•" are used to enter new parameter values. A maximum of 10 digits are allowed for frequency data and 3 digits for amplitude. When a volt terminator (Volt or mV) is to be used, only the first two significant digits are used to generate the amplitude. When the dBm terminator is to be used, up to three digits are used (amplitude ≥10.0 dBm).

3.4.4 Terminator Buttons

The terminator buttons are: MHz/dBm, kHz/Volt and Hz/mV. Most parameters (commands that require a numeric entry) are first entered into a scratch pad memory, then transferred to the synthesizer output circuitry when the terminator button is pressed. (See paragraph 3.4.6 for use of the terminator buttons in parameter entry.)

The GPIB Address parameter button does not require a terminator. Data for the GPIB Address parameter is always entered as two digits and the data becomes valid when the second digit is entered.

3.4.5 Errors

Attempting to enter a value outside the legal limits of the selected parameter will result in a blinking display when the terminator button is pressed. The last valid data entry for this parameter will remain in effect. In addition, if the maximum number of digits allowed for a parameter is exceeded (10 for frequency, 3 for amplitude, and 2 for GPIB Address), the display will blink before the terminator button is pressed.

The blinking display is cleared with the Clear button (section 3.4.1.2) or if the parameter buttons (section 3.4.2) are pressed. In either case, the last valid numeric value for the selected parameter is then displayed.

3.4.6 Parameter Entry

There are two basic methods of entering parameter values:

1. Select the desired parameter, enter the necessary numeric value, and terminate the number with the proper terminator button (unless GPIB Address was selected).

   Example: Ampl 1 0 . 3 dBm

   causes an immediate amplitude change to 10.3 dBm (if not already at 10.3 dBm).

2. Select the desired parameter, then press the Display Modifier "On" button to activate the blinking digit. Use the Select Digit buttons, ► or ◄, to select the proper digit. Now use the Modify Digit, ▲ or ▼, to increment or decrement the value.

The use of the Display Modifier buttons will cause an immediate execution of the change. If this is undesirable, the synthesizer output should be first disabled by pressing the RF Output On button (button light extinguished). To continuously change the parameter value, hold down the ▲ or ▼ buttons.

Data is shifted into the display with the correct number of digits or zeroes after the terminator button has been pressed. The following example illustrates how data is entered into the synthesizer. The initial condition is the default or power-up state.

Keystrokes	Resulting Display
Freq	250,000,000.0
1234.56789	12,345,678
kHz	1,234,567.8

Notice that as the numeric data is being entered, commas are automatically displayed to separate the MHz, kHz, and Hz positions on the display. Since these commas are hardwired and cannot be controlled by the front panel, the commas and the decimal point may appear to be in the wrong location until a terminator button is pressed.

NOTE

An error will occur, if more digits are entered than can be displayed in the readout.

3.5 INTERFACE PRIORITY

Since both the GPIB (option 06) and BCD interfaces may be installed together, the BCD interface takes priority over the GPIB interface in both the 5155A and 5156A. Remote enable lines for each interface (pin 42 on the BCD and pin 17 on the GPIB) are used to notify the synthesizers that the specific interface is active. If the remote enable line of the BCD interface is active and the instrument is connected to the GPIB with its remote enable true (typical GPIB statement like "REN @7" will make remote enable line true), the BCD interface takes control and the GPIB interface drivers on the synthesizer are disabled.

CAUTION

It is not recommended that both interfaces be connected at one time. If both cables are connected, ensure that there is no data activity on the unused interface. Data activity on the unused interface may cause unexpected results on the active interface.

3.6 REMOTE BCD OPERATION

3.6.1 Introduction

Connectors

The BCD remote programming interface is standard on Models 5155A and 5156A. Remote BCD control of frequency through the 50-pin rear panel connector is essential for those applications demanding very fast frequency switching. Remote control of amplitude is through the 14-pin rear panel connector.

Double Buffering

All frequency and amplitude data lines are double buffered. This two stage buffering ensures that new data can be synchronously switched from one state to another.

Connections and Programming

Two types of connections and programming are discussed: "all digits simultaneously" or "digit pairs". The latter for programming byte serially from a microcomputer data bus.

Switching Transient, Program Delay and Phase Continuity

Review specifications in section 1. These characteristics are discussed here.

3.6.2 BCD Interface and Programming

The 50-pin rear panel connector remotely controls the synthesizer frequency in 0.1 Hz steps throughout the 1 to 999.999 999 9 MHz range. The 14-pin rear panel connector remotely controls the amplitude setting in 0.1 dBm steps throughout the + 3.1 dBm to + 13.0 dBm range. Pin-out details for the 50-pin frequency connector are given in table 3-3, and for the 14-pin amplitude connector, in table 3-4.

Double buffering provides storage of each frequency and amplitude digit so if several digits are to be kept constant, data for those digits does not have to be continuously supplied. Only data for those digits to be changed has to be supplied.

All clock and data signals are TTL compatible. Negative-true logic is employed on all data lines. Logical "1" is from 0.0 to 0.8 volts and logical "0" is from 2.0 to 5.5 volts. All lines are referenced to ground (pin 50 on the 50-pin connector, and pins 2, 3, 13 and 14 on the 14-pin connector). Pull up resistors are used so a line left unconnected will assume a logical "0" condition. A contact closure may be used, therefore, to ground desired lines for logical "1" and left open for logical "0".

All data lines, register strobes and execute strobe (see tables 3-3 and 3-4) represent one low power Schottky (LS) TTL load.

After the input BCD data has settled, a rising edge of the first buffer register strobe will store the data into the first rank of buffers. The data may now be removed from the bus. A rising edge of the execute strobe (pin 43 on the 50 pin connector) no sooner than 200 ns after the rising edge of the register strobe will clock the data into the second rank of buffers in the synthesizer to start the change of frequency and amplitude.

Note

The execute strobe line should be disconnected or held between 2 and 5.5 Vdc when being programmed from the GPIB.

Table 3-3. BCD Frequency Programming Connections

	Connector Pin Number				
	BCD Weight				
Digit	1	2	4	8	Register Strobe First Buffer
100 MHz	49	48	45	44	23
10 MHz	15	16	40	41	23
1 MHz	17	18	19	20	24
100 kHz	1	2	26	27	24
10 kHz	3	4	28	29	25
1 kHz	5	6	30	31	25
100 Hz	7	8	32	33	46
10 Hz	9	10	34	35	46
1 Hz	11	12	36	37	47
0.1 Hz	13	14	38	39	47

	Pin
Remote Enable:	42
Remote Enable Ground:	50
Execute Strobe:	43

NOTE: 1. 50 pin mating connector: Cinch 57-30500 (Wavetek P/N: 351.5001).
2. All functions above are negative-true logic.
3. Freqeuncy changes on rising edge of execute strobe.

3.6.2.1 Remote Programming — All Digits Simultaneously

If the application allows simultaneous programming of all synthesizer control lines, connect the data lines individually as indicated in tables 3-3 and 3-4. All first buffer register strobe lines may be tied together (pins 23, 24, 25, 46 and 47 on the 50-pin connector, and pin 1 on the 14-pin connector). The delay from the rising edge of the register strobe to the rising edge of the execute strobe should be no sooner than 200 ns.

3.6.2.2 Remote Programming — Digit Pairs

When the application does not require simultaneous programming of all frequency control lines, the following technique may be used to enter data from a microcomputer data bus in byte serial fashion. Because double

buffering is used, the phase continuity of the 0.1 Hz to 10 kHz digits is maintained using this technique.

For entering data in byte serial fashion (refer to tables 3-3 and 3-4) hardwire the bit weights of every other digit together so that only two lines drive each bit. For example, to hardwire the "1" bit weight, short pins 49, 17, 3, 7 and 11 together, then connect one lead (which will be called "A" for this discussion) from these pins to the BCD controller. Also short pins 15, 1, 5, 9 and 13 together, again connecting one lead (called "B") to the BCD controller. Duplicate this procedure for weights "2", "4" and "8". Independently connect all register strobe lines to the controller.

Table 3-4. BCD Amplitude Programming Connections

	Connector Pin Number				
	BCD Weight				
Digit	1	2	4	8	Register Strobe First Buffer
1 dB	8	9	7	6	1
0.1 dB	10	11	5	4	1

Remote Ground: Pins 2,3,13,14
Execute Strobe: Pin 43 on 50-pin connector

NOTE: 1. 14-pin connector: Amphenol 57-30140 (Wavetek P/N 351.1401)
2. All functions above are negative-true logic.
3. Amplitude changes on rising edge of execute strobe.
4. Amplitude is programmed in attenuation from full scale (+ 13.0 dBm).

Suppose the following data is to be programmed into the synthesizer; pin 49 "0" (high), pin 15 "1" (low), pin 17 "1" and pin 1 "0". To latch data at pins 49 and 15 into the first set of buffers, bring lead "A" high (0) and "B" low (1), then pull pin 23 (register strobe) high. To latch data at pins 17 and 1, bring lead "A" low (1) and "B" high (0), then pull pin 24 (register strobe) high. Duplicate this process for the remaining bits, then strobe the execute line high (pin 43 on the 50-pin connector) to enter the data into the working registers.

If only the digits **below** the 100 kHz digit have been changed, the output frequency will maintain phase continuity.

3.6.2.3 Remote BCD Amplitude Programming

Amplitude is programmed in the same manner as frequency except that the programming data lines are located on the 14-pin connector. The first buffer register strobe stores the data in the first rank of buffers. The execute strobe on the 50-pin connector loads the amplitude data into the working register in order to initiate the change. The synthesizer powers up at full scale (+ 13 dBm). If the unit is powered up in remote BCD, a buffer and execute strobe will be required to set the amplitude to a known level.

3.6.3 5155A Local/Remote Considerations

To send frequency or amplitude data on the BCD bus, the remote enable line (pin 42) must be active (low). When this occurs, the front panel controls are disabled, and the front panel Locked Out LED and BCD Active LED illuminate. Front panel control is restored when the remote enable line (pin 42) is released (high). (Also see GPIB operation.)

The display will remain active even though the synthesizer is being controlled by the BCD interface. If data updates come less than 0.5 seconds apart, the display will skip some values; however, the synthesizer will continue to keep pace with the data inputs.

Data entered from front panel pushbuttons is maintained when the remote enable line is **first** pulled low (to go into the BCD mode). If a load pulse is sent to the execute strobe line (pin 43), any data present in the first rank of frequency buffers will be loaded into the synthesizer.

When the remote enable line (pin 42) is released and front panel control is restored, the last frequency and amplitude values sent over the BCD interface will be displayed on the LCD readout.

3.6.4 5156A Special Considerations

The 5156A powers up with the BCD LED lit unless the GPIB interface is connected and activated. See paragraph 3.7. If the unit powers up in BCD mode, an arbitrary frequency setting will result unless the synthesizer is initialized. This is done by supplying frequency data to the BCD programming lines and loading it with the register strobes and execute strobe as described in paragraph 3.6.2.

3.7 REMOTE GPIB (IEEE-488) OPERATION

3.7.1 Introduction

Model 5155A and Model 5156A may be remotely controlled via the General Purpose Interface Bus (GPIB) if Option 006 is ordered. To remotely control these instruments:

1. Connect the instrument to the GPIB system with the standard GPIB cable and connector. (See section 2.2.4.)
2. Set the instrument GPIB address to a unique device identification number (between 0 and 30) with the rear panel dip switches or the front panel GPIB Address button. (See section 2.2.5.)
3. Activate the GPIB interface and interface drivers in the synthesizer by asserting the remote enable (REN) line (i.e., pull low). The following commands may be used by the Wavetek 6000 Instrumentation Controller to explicitly assert the remote enable line on the GPIB:

   REN @7
   REN @707

4. Remotely program the instrument with the ASCII control codes over the GPIB.

NOTE

The display of the Model 5155A will remain active even though the synthesizer is being controlled by the GPIB interface. Since the GPIB interface can change either frequency or amplitude every 125 ms, and the display can only update every 500 ms, it will appear that some steps are skipped if the maximum update rate is used. The display will be skipping some values but the synthesizer will still be switching the output at the desired rate.

3.7.2 ASCII Control Codes

3.7.2.1 Model 5155A

The remote control ASCII characters for the 5155A are listed in appendix B. Please note that:

1. Some of the commands available to the Model 5155A are not permissible for the Model 5156A. (The commands for the Model 5156A are listed separately in the Programming Command Summary in appendix C.) A rear panel switch (No. 7) on the Model 5155A may be used to **force** the user to program the 5155A **only** with the commands that are acceptable to the 5156A so that programs for the 5156A may be developed on the 5155A compatability mode.
2. Some characteristics of the compatibility mode on the 5155A are:
   a. If the 5156A mode on the 5155A is selected with switch No. 7, only the primary commands listed in appendix C for the 5156A are allowed and must be spelled correctly for the portion of the command that is used.
   b. Other characters or commands not in this list generate an SRQ to signify that the command is unrecognizable.
   c. A space is needed between the primary command (F or A) and the numeric value. If a numeric modifier is used (e.g., MHZ or KHZ), no space is needed after the number.
3. Not all front panel keys have a directly equivalent remote control command. These keys are:

   GPIB Address
   Cursor (▲,▼,◄,►)
   Clear

4. Not all remote control commands have a directly equivalent front panel key. These commands are:

   Execute (EXECUTE)
   Revision (REV)
   Command Recall (RECALL)
   State of Instrument (STATE)
   Help (HELP)

5. All commands must be sent over the GPIB as upper case or capital letters with the exception of the m for milli and e for exponential notation. The upper case M is for mega. Either the e or the E may be used for the entry of data in scientific notation. An SRQ is generated if lower case letters other than an m or e are used.
6. Most of the commands may be sent over the GPIB either as the full spelling of the command or as a shortened version. In any case, the correct spelling of the command must be used or an SRQ is generated and the command is not accepted. Examples of these types of commands are:

   FREQUENCY (F)
   AMPLITUDE (A)
   EXECUTE (E)
   RECALL (REC)

7. Some commands require two words to complete the command. A primary command describes the general function and a secondary command describes what allowable portion of this function is to be used. These commands are:

   RF ON
   RF OFF

MODIFY UP
MODIFY DOWN
MODIFY LEFT
MODIFY RIGHT
MODIFY ON
MODIFY OFF
VIEW FREQUENCY
VIEW AMPLITUDE
VIEW ADDRESS

3.7.2.2 Model 5156A

The remote control ASCII characters for the Model 5156A are listed in appendix C. Please note that:

1. No execute command is required at the end of a data transfer (as it is in the Model 5155A.)
2. Only frequency and amplitude are programmable, and the 5156A does not support a talker capability.
3. All commands must be sent over the GPIB interface as capital letters.
4. Any characters not part of the command list for the 5156A will be ignored.

NOTE

Programs become easier to understand when additional characters are used. For example, the command "F123456789.0" is more meaningful as "FREQ123.456, 789MHZ".

NOTE

A space between the primary command and the numeric value is ***not*** *needed for the 5156A and will not generate any errors. It is needed in the 5156A compatibility mode on the 5155A. No errors will be generated if a program is developed on the 5155A for use on the 5156A since the space will be ignored on the 5156A. In addition, an SRQ will be generated on the 5155A (in 5156A compatibility mode) if commands are spelled incorrectly, even though any extraneous characters will be ignored in the 5156A.*

5. Only the following commands are recognized by the 5156A:

   F Frequency
   A Amplitude
   M MHz
   K kHz

6. No modifiers for the numeric value are required. Frequency is assumed to be in Hz if the MHz or kHz modifiers are not used and amplitude is always assumed to be in steps of 0.1 dB from +3.1 dBm to +13.0 dBm.

3.7.3 Differences Between Controllers

GPIB control commands have not, as yet, been standardized for any computer language such as BASIC or PASCAL and will vary from one controller manufacturer to another. For example, the Wavetek 6000 Instrumentation Controller uses a WRITE statement to send information to the instrument while another manufacturer may use an OUTPUT statement. Consult your controller manual for the proper controller commands. The GPIB commands and sample programs in this manual are written using the Wavetek 6000 Instrumentation Controller, and with the 5155A and 5156A GPIB addresses set to 07.

3.7.4 The End of String (EOS) or Terminator Character

3.7.4.1 Model 5155A

An EOS character has two uses. During input to the synthesizer (i.e., WRITE statements), it signals the end of a group of programming characters. During output from the synthesizer (i.e., READ statements), it is appended to the end of every response to a talk request on the GPIB. Since it is always recognized, even in a quoted string, it can be used to ensure that the instrument is in a known state by ending any possibly pending commands on the GPIB so that new commands, when begun, are interpreted correctly.

An EOS character for any data sent to the synthesizer is a Carriage Return (CR), which is decimal 13, and a Line Feed (LF), which is decimal 10.

Both the CR character and the End or Identify (EOI) line are used by the synthesizer to signify the end of a talk message. The system controller may sense either of the conditions to determine when the transfer has been completed.

3.7.4.2 Model 5156A

The 5156A differs from the 5155A in the EOS character that is used. Only the Carriage Return (CR), which is decimal 13, is used to signal the end of the ASCII characters being sent in the listen mode. There is no talk capability for the 5156A.

3.7.5 Sending GPIB Instrument Commands

The controller handles the function of controlling the handshake or bus management lines such "attention" or "unlisten". To send GPIB commands to the 5155A and 5156A, it is only necessary to determine which ASCII commands are necessary to perform the desired action on the synthesizer.

For example, to set the 5155A amplitude level to +10.3 dBm, a possible command is WRITE @707: "A 10.3DB". This command sends the ASCII characters "A 10.3DB" via interface No. 7 to the instrument designated as device No. 07.

NOTE

The programming commands for the Model 5156A are a subset of the Model 5155A commands. Refer to appendix C for a complete listing of the allowable commands for each instrument. See section 3.7.2.1 items 1 and 2 for a brief discussion on how the command list of the 5155A may be reduced to that of the 5156A.

Alphabetic and numeric characters must be sent enclosed in quotation (") marks or as an alphanumeric (string) variable such as A$. Numeric characters (1,2,13,...) may be sent as a numeric value or a numeric variable (X).

For example, if the numeric variable X contains the value 10.3 and the alphanumeric variable A$ contains the ASCII characters A 10.3DB, then the following commands for the 5155A (and in a similar fashion for the 5156A) are all equivalent:

5155A	**5156A**
WRITE @707: "A 10.3DB"	WRITE @707: "A10.3"
WRITE @707: "A", 10.3, "DB"	WRITE @707: "A103" (".") not needed)
WRITE @707: "A", X, "DB"	WRITE @707: "A"; X
WRITE @707: A$	WRITE @ 707:A$ (DB is ignored)

3.7.5.1 EXECUTE Command

The execute command is used to cause the output of the 5155A (not needed on the Model 5156A) to change to a new value. The carriage return (decimal 13) causes the 5156A to change to its newly programmed value. Please note that:

1. Until the execute command is sent, only the display of the 5155A is changed. This enables the user to synchronize the change of the output when both frequency and amplitude are altered without causing the output to go through an intermediate step. An example of this command would be:

   WRITE @707: "FREQ 125.9876M"
   WRITE @707: "AMPL 12.5DB"
   WRITE @707: "EXEC"

2. The RF Output command is immediately executed and does **NOT** require that an execute command be sent.

3.7.5.2 GET Command

While the execute command can be used to synchronize all changes in the 5155A, the GET command is used to synchronize several different instruments connected on the GPIB. There are some differences in the implementation of the GEt command for both the 5155A and the 5156A. Please note that:

1. The GET command is used in place of the execute command for the 5155A if more than one instrument must be synchronized for some action. The display of the 5155A will change when the commands are received but the output will not change until either the GET or execute command is sent.
2. Even if the 5155A and controller are the only instruments connected on the GPIB, the GET command can be used to cause the 5155A to implement the programming changes. It is equivalent to issuing the execute command in this instance.
3. In the 5156A, the carriage return (decimal 13) is used to load the programming information into the frequency and amplitude generation circuits. When it is desired that the 5156A change its output in synchronization with other instruments, no carriage return must be sent to the 5156A. It is often automatically sent as the terminator to a command message, so a format statement must be used to prevent the carriage return from being sent. An example of such a statement is:

   WRITE @707: "F 545.43M", (";" inhibits terminator)

   or

   TERM is "" (sets terminator to null)
   WRITE @707: "F 545.43M"
   TERM is CHR$(13) & CHR$(10) (sets terminator to CR & LF)

3.7.5.3 Concatenating Multiple Commands

Sometimes it is desirable to join (concatenate) separate commands into one command statement. The "at" character (@) is used in the 5155A to join multiple commands into one statement.

1. The 5156A does not require the use of the "@" character since both frequency and amplitude may already be programmmed in one statement. If the "@" character is used in the 5156A compatibility mode (see section 3.6.2.1 items 1 and 2), it will be ignored. Thus, multiple command statements developed on the 5155A for use in the 5156A are allowed.

2. A space is required both before and after the "@" character.
3. The "@" character may be used as many times as desired as long as the maximum number of characters (48) allowed in the command statement is not exceeded.

3.7.6 Reading Instrument Responses

Except for the SRQ line, the instrument will not transmit data on the bus until it is commanded to do so by the controller. The two ways that a controller can request information from the synthesizer are with a poll request (either serial or parallel) or a talk command.

3.6.6.1 Talk Command

NOTE

Only the Model 5155A is capable of entering the talk mode on the GPIB. The Model 5156A is a listen only device designed for high speed data transfers.

The controller requests information from the instrument by first sending the proper command to the instrument while the instrument is in the listen mode. The instrument, recognizing that this command is requesting information, becomes a talker and sends data back to the controller. The controller used for these examples utilizes a READ statement to receive information from the instrument.

```
READ @707: A$
```

The data is then placed in an alphanumeric variable. Other controllers might use statements such as INPUT commands to read data from a device. Please consult your controller's operating manual for details on data transfers.

What the instrument will say when it is addressed to talk depends on the command **prior** to the READ statement. The change of the instrument from a listener to a talker and the selection of the type of data to be transferred is accomplished automatically when any of the following commands are sent:

```
HELP
RECALL
REV
STATE
```

These are now explained in more detail.

3.7.6.1.1 HELP Command

The HELP command in the 5155A provides a complete listing of GPIB programming commands so that references back to a written manual can be avoided. The list of commands are read by the controller as a single alphanumeric (string) array of approximately 500 characters. The following is taken from a sample demonstration program in this manual:

```
DIM HELPLIST$*500
WRITE @707: "HELP"
READ @707: HELPLIST$
```

Refer to section 3.7.7 table 3-6 for sample demonstration program which reads the HELP command list and separates each command for easier display and use.

3.7.6.1.2 RECALL Command

The RECALL command allows the user to read the previous ASCII command that was sent over the GPIB. This is a very useful feature for program debugging since it allows the programmer to read the last statement that caused a service request to be generated. This can pinpoint spelling and typing mistakes very quickly.

When an SRQ (section 3.7.6.2) is generated by an incorrect statement in a program, the RECALL command may be used to troubleshoot the problem in one of two possible ways. A simple approach would be to reset all equipment in the system and then single step the program. When the SRQ LED on the front panel becomes illuminated, the RECALL statement can be manually issued from the controller's keyboard to read the command statement in question.

In a more elaborate scheme, a subroutine may be used to automatically issue the RECALL statement when an SRQ is generated by the 5155A (refer to your controller's operating manual). The incorrect command can then be viewed on the controller's display for correction.

The maximum length of the alphanumeric variable that is transmatted to the controller is 48 bytes or characters. The command is issued as follows:

```
WRITE @707: "FREQ 1257 kH"
WRITE @707: "RECALL"
READ @707: COMMAND$
```

The contents of COMMAND$ is "FREQ 1257 kH". A service request was Generated because the logic in the synthesizer was not able to recognize the lower case "k" in the command (only upper case letters are allowed.) The corrective action would be to capitalize the "k" and re-enter the statement into the program.

3.7.6.1.3 REV Command

The REV command returns a single alphanumeric character to the user to identify the current revision

level of the software located in PROM (Programmable Read Only Memory). This command may be used as follows:

```
WRITE @707: "REV"
READ @707: REV$
```

where REV$ contains one ASCII character (i.e., "A" for first level).

3.7.6.1.4 STATE Command

The STATE command allows the user to read the current status of the 5155A display. Since the synthesizer's display can be updated before the actual change in frequency or amplitude is activated (with the EXECUTE command), the STATE command shows the last parameter entered even if it has not been executed.

NOTE

The output of the 5155A will ***not*** *change until a GET (Group Execute Trigger) or execute comand is sent. Refer to sections 3.7.5.1 and 3.7.5.2.*

Three conditions of the 5155A are read by the STATE command (frequency, amplitude, and RF output status) into a single alphanumeric (string) array of 32 characters long (maximum). The following example illustrates the use of this command:

```
WRITE @707: "STATE"
READ @707: INSTR_STATE$
```

3.7.6.2 Polling

The 5155A's SRQ signals the controller that the 5155A requires attention. It is always active and does not have to be explicitly turned on by the 5155A like the talk mode. Most controllers, however, do require that the SRQ capability for the controller be enabled before an SRQ can be detected. An SRQ usually occurs whenever an error condition exists in the 5155A and the 5155A wishes to alert the user of a possible problem. These problems may be incorrectly spelled commands, data out-of-range, illegal characters, too many characters, etc. Since the SRQ line is common to all devices, additional tests must be made to determine which device or devices are signaling for attention. Both serial and parallel polling accomplish this.

3.7.6.2.1 Parallel Poll

The parallel poll is an extremely fast technique for interrogating bus device status since all devices on the bus are interrogated at once. In a parallel poll, the controller assigns each device (up to 8) a unique bit with the parallel poll configure (or enable) command (refer to your controller's operating manual.) When a parallel poll is performed as a response to the SRQ being asserted by one or more devices, the controller reads the parallel poll status word from each instrument. The condition of each bit in the word tells the controller which device or devices have requested service. Should a device not request service, it does not activate its specific bit in the parallel poll status word.

PPE @707:1,1 — Controller configures 5155A to set bit 1 (second bit) high (1) when it requests service.

PPL @7:X — Perform parallel poll and read status byte into numeric variable, X, where second bit of X = 1 if the 5155A has requested service.

The controller then performs a serial poll on all devices responding to the parallel poll to determine the specific message of each device.

3.7.6.2.2 Serial Poll

The information obtained from reading a serial poll register is device dependent and each manufacturer determines what information should be made available to the user. A serial poll may be performed either randomly or as a result of a subroutine monitoring the SRQ line. If a parallel poll were initially performed, then the devices requesting service would be known. If, however, some of the devices do not provide parallel polling capability, a serial poll on each device would have to be performed until it is determined that there are no devices still requesting service (ASK @ command for the Wavetek 6000.)

Once a service request has been detected (refer to your controller's operating manual), the following command can be used to read the status:

```
STATUS @707:GPIB_STATUS
```

where GPIBSTATUS is greater than 64 if the 5155A has requested service.

Table 3-5 shows the serial poll response byte. Each of the 7 bits represents a condition that gives additional information concerning the present status of the synthesizer. Bit 6, decimal 64, tells the controller that service has actually been requested.

3.7.7 Sample Demonstration Programs

Because each test system is unique and controller programming commands are not standardized, it is impossible to provide actual application programs in this manual. The following sample demonstration programs were written for the Wavetek 6000 Instrumentation Controller controlling a single instrument (the Wavetek 5155A-006), and demonstrate instrument control, read back from the instrument, SRQ and polling. The programs also demonstrate some of the Wavetek extensions of the BASIC computer language: program labels, DO loops, and unlimited length variable names. In all programs, the 5155A GPIB address is set to 6. The programs are presented as tables containing both the actual program statements and explanatory comments.

Table 3-5. Serial Response Byte

Bit Binary Position	Bit Decimal Value	Bit Name	Bit Description
1000 0000	128 (MSB)	—	Not used
0100 0000	64	SRQ	Indicates request for service
0010 0000	32	—	Not used
0001 0000	16	COMPATBL	Commands not allowed for 5156A compatibility mode (section 3.7.2.1)
0000 1000	8	OUT OF RNG	Data out of range for frequency and amplitude
0000 0100	4	—	Not used
0000 0010	2	OVERFLOW	Greater than 48 characters in command string
0000 0001	1 (LSB)	SYNTAX	Unrecognizable command

Table 3-6 contains a simple program to read the HELP command list contained in the internal memory of the 5155A. This program separates each command for easier viewing and lists all allowable GPIB statements for the 5155A.

Table 3-7 contains a simple program to sweep the 5155A between two fixed frequencies.

Table 3-8 contains a simple program demonstrating the use of the DISPLAY MODIFIER section in the 5155A. It will set up the 5155A to a given frequency and amplitude and then use the DISPLAY MODIFIER increment command to manually sweep the output frequency.

Table 3-9 contains a more advanced program to demonstrate the use of the SRQ capabilities of the 5155A. Both the parallel and serial poll features are used to determine if the 5155A was the instrument that requested service of the controller and what was the cause of the request.

Table 3-6. Sample Demonstration Program — "HELP"

Program Statements	Explanation
100 ! PROGRAM — HELP	Comment statement containing program name.
110 DIM HELP$*500	Set length of alphanumeric string variable for maximum expected number of characters.
120 Dev_Adrs = 707	Set device address (Dev_Adrs) for interface 7 and instrument at address 7.
130 CLEAR	Clear controller screen.
140 WRITE @Dev_Adrs: "HELP"	Send alphanumeric characters to device specified as Dev_Adrs.
150 READ @Dev_Adrs: HELP$	Command instrument at address Dev_Adrs to talk. Place received data in alphanumeric string variable, HELP$.
160 P = 0	Set pointer, P, to 0.
170 P1 = POS (HELP$, "]" P)	Calculate location of first occurrence of a "]".
180 WRITE @0: HELP$(P + 1:P1)	Display portion of HELP command on controller screen.
190 WRITE @0	Display blank line on controller screen.

Table 3-6. Sample Demonstration Program — "HELP" (Continued)

Program Statements	Explanation
200 P = P1	Reset pointer to end of displayed portion of HELP$.
210 DO UNTIL P1 = 0	
220 P1 = POS(HELP$, ";", P + 1)	Calculate each location of ";" which separates commands.
230 WRITE @0: HELP$(P + 1:P1)	Display next portion of HELP command.
240 P = P1	Reset pointer to locate next occurrence of ";".
250 LOOP	End loop to separate commands in HELP list.
260 END	End of program.

Table 3-7. Sample Demonstration Program — "SWEEP"

Program Statements	Explanation
100 ! PROGRAM — SWEEP	Comment statement containing program name.
110 Dev_Adrs = 707	Set device address (Dev_Adrs) to interface 7 and instrument at address 7.
120 START = 125.735	Set start frequency variable to 125.735 MHz.
130 STOP = 132.678	Set stop frequency variable to 132.678 MHz.
140 STEP = 0.125	Set sweep step size to 125 kHz.
150 F = START	Rename START for use in WRITE statement.
160 WRITE @Dev_Adrs: "A 13.0DB"	Send command for amplitude of +13.0 dBm to Dev_Adrs (interface 7 instrument address 6).
170 DO UNTIL F > STOP	Start loop to sweep 5155A. Loop will be terminated when variable F is greater than variable STOP.
180 WRITE @Dev_Adrs USING "C4, X, F7.3, C5": "FREQ", F, "MHZ E"	Send frequency data to 5155A.
190 F = F + STEP	Calculate next frequency.
200 LOOP	End sweep loop.
210 END	End of program

Table 3-8. Sample Demonstration Program — "DISPLAY MODIFIER"

Program Statements	Explanation
100 ! PROGRAM — DISPLAY MODIFIER	Comment statement containing program name.
110 Dev_Adrs = 707	Set device address (Dev_Adrs) to interface 7 with instrument at address 7.
120 WRITE @Dev_Adrs: "FREQ 789.532 MHZ"	Send command to 5155A to change frequency to 789.532MHz.
130 WRITE @Dev_Adrs: "AMPL 12.7DB"	Send command to 5155A to change amplitude to +12.7 dBm.
140 WRITE @Dev_Adrs: "EXEC"	Send command to implement parameter changes.
150 WRITE @Dev_Adrs: "MODIFY ON"	Send command to cause rightmost digit to begin blinking.
160 FOR I = 1 TO 4	Start loop to move blinking digit to 1 kHz position.
170 WRITE @Dev_Adrs: "MOD LEFT"	Send command to move blinking digit one location to the left.
180 NEXT I	End loop.
190 DO	Start of endless loop to increment frequency (no WHILE or UNTIL condition is specified).
200 WRITE @Dev_Adrs: "MOD UP"	Send command to increment blinking digit by 1.
210 . . .	Additional statements — read power meter for instance.
220 LOOP	End loop to continuously increment 1 kHz digit.
230 END	End of program.

Table 3-9. Sample Demonstration Program — "POLLING"

Program Statements	Explanation
100 ! PROGRAM — POLLING	Comment statement containing the program name.
110 Dev_Adrs = 707	Set device address (Dev_Adrs) to interface 7 with instrument at address 7.
120 CLEAR	Clears controller screen.

Table 3-9. Sample Demonstration Program — "POLLING" (Continued)

Program Statements	Explanation
130 PROCESS EVENT SRQ "@07,02"	Defines the interrupt to be Bit No. 2 on interface No. 7. The interrupt name is SRQ.
140 START GPIB__POLL	Instructs the parallel process named GPIB__POLL to begin.
150 CONNECT EVENT SRQ	Enable interrupt capability on SRQ.
160 AMP = 12.0	Set variable to 12.0 (dBm).
170 PPE @Dev__Adrs: 3, 1	Configure Dev__Adrs (5155A) to set bit No. 3 true in parallel poll register when requesting service.
180 WRITE @Dev__Adrs: "AMP 12.0DB E"	Send command setting 5155A to +12.0 dBm.
190 WRITE @Dev__Adrs: "MODIFY ON"	Send command causing rightmost digit (0.1 dB) to blink.
200 WRITE @0: "Amplitude is +12.0 dBm"	Display message on controller screen.
210 DO	Start endless loop to increment amplitude.
220 WRITE @Dev__Adrs: USING "C3,X,F4.1,C2": "AMP",AMP,"DB"	Send command to change amplitude.
230 BEEP 2000,100	Generate audible beep from controller.
240 AMP = AMP + 0.1	Increment amplitude by 0.1 (dB).
250 WRITE @0: "Amplitude is +", AMP, "dBm"	Display new amplitude level on controller screen.
260 LOOP	End loop to continuously increment amplitude.
270 END	End main program.
280 PARACT GPIB__POLL URGENCY 50	Beginning of parallel process that watches for an SRQ. Has higher priority than main program.
290 WAIT EVENT SRQ	Statement that watches for an SRQ.
300 PPL @7:P__POLL	Perform parallel poll and read status byte into P__POLL.
310 IF BIT(3, P__POLL) THEN GOTO SERIAL__POLL	Check if 5155A requested service. If yes, then perform serial poll routine.
320 WRITE @0: "SRQ NOT GENERATED BY 5155A"	Display message on controller screen.

Table 3-9. Sample Demonstration Program — "POLLING" (Continued)

Program Statements	Explanation
330 END PARACT	End parallel program.
340 SERIAL__POLL:	Program label for serial poll subroutine.
350 WRITE @0	Display blank line on controller screen.
360 WRITE @0: "Cause of SRQ is"	Display message on controller screen.
370 STATUS @Dev__Adrs: S__POLL	Perform serial poll on instrument at Dev__Adrs and read status byte into S__POLL.
380 IF BIT(0, S__POLL) THEN WRITE @0: "Syntax Error"	Display message on controller screen.
390 IF BIT(1, S__POLL) THEN WRITE @0: "Command String Overflow (>48 chars)"	Display message on controller screen.
400 IF BIT(3, S__POLL) THEN WRITE @0: "Data Out of Range"	Display message on controller screen.
410 IF BIT(4, S__POLL) THEN WRITE @0: "Command Not Allowed in 5156A Mode"	Display message on controller screen.
420 END PARACT	End parallel program.

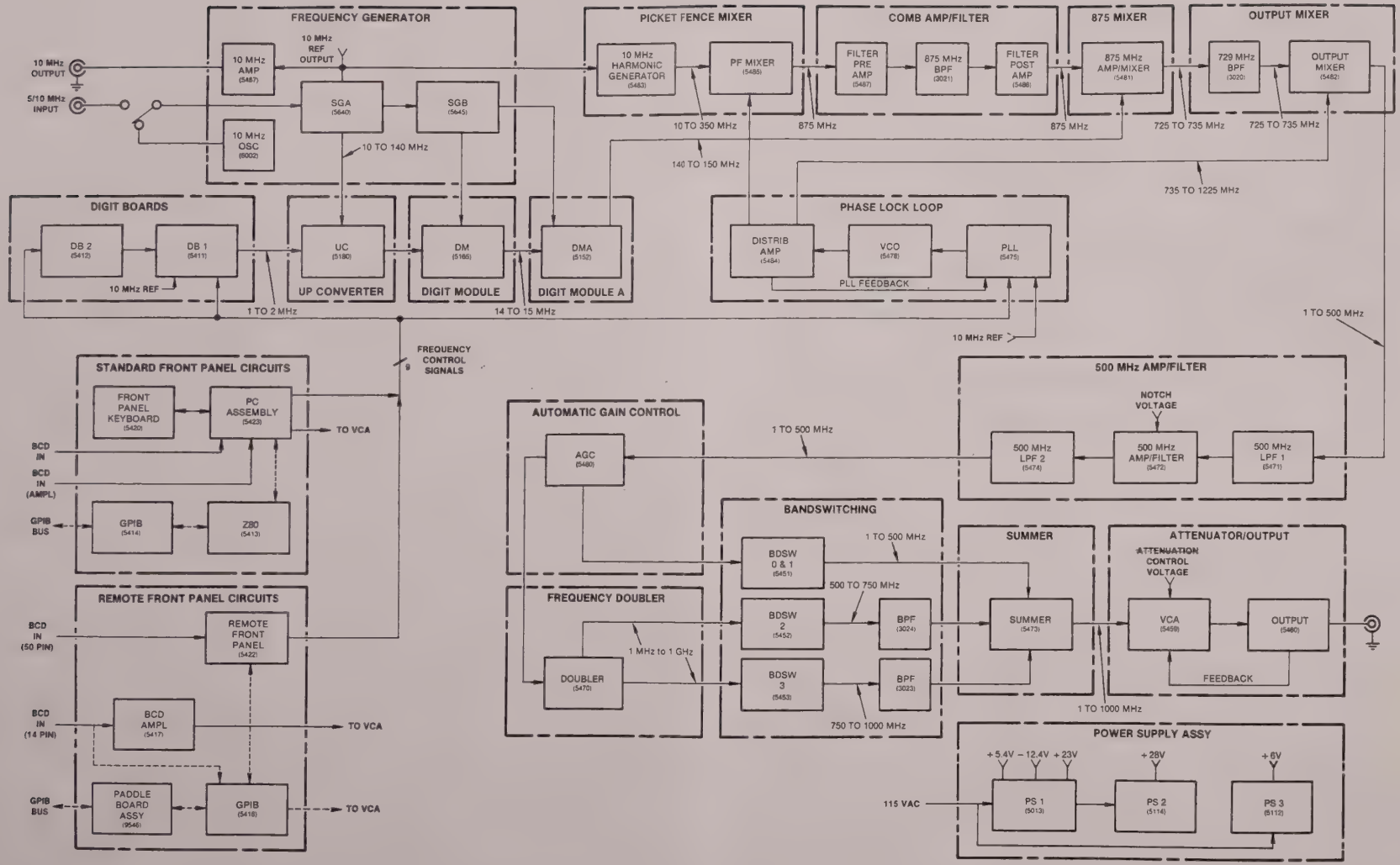


Figure 4-1. Functional Block Diagram

SECTION 4
THEORY OF OPERATION

4.1 GENERAL CIRCUIT DESCRIPTION

All of the synthesizer output frequencies are derived from a crystal oscillator by arithmetic operations and are fully coherent with the reference standard. A 10 MHz pulse, whose spectrum is a frequency "comb" from 10 to 350 MHz, is used to generate the auxillary fixed frequencies needed by the instrument. Fine resolution steps are produced using a direct digital synthesis for steps below 10 kHz. The 100 kHz and 1 MHz digits use direct analog circuits that contain mixers and dividers for these steps of resolution. A wide band translator circuit is used for the 10 and 100 MHz steps of resolution. A frequency doubler, three bandswitching circuits, and a summer extend the range to 1 GHz.

4.2 FUNCTIONAL BLOCK THEORY

All of the modules or boards have been grouped into functional blocks (refer to figure 4-1) that contain one or more modules or boards. The blocks are arranged in a control signal/output signal order. Each of these functional blocks is then discussed in general. A more detailed description of each module or board can be found in sections 6 through 25 along with maintenance information, troubleshooting, parts lists, and schematics.

4.3 FRONT PANEL/CONTROL CIRCUIT FUNCTIONAL BLOCK

The local and remote circuits are described in two different paragraphs in order to highlight the differences between the Model 5155A (standard or local version) and the Model 5156A (remote version).

4.3.1 Model 5155A Front Panel/Control Circuits

The front panel/control circuits for the Model 5155A consist of a keyboard assembly, a front panel PC assembly, a Z-80 board, and if the IEEE-488 option is specified, a GPIB "paddle board" assembly.

Keyboard Assembly

The keyboard assembly contains the manual control input keys, keyboard encoder, display controller, latches, and the liquid crystal display. The control input keys allow the user to input control data which is then routed directly to the internal control bus and to the display controller. If there is an external BCD input, that control data is input via the front panel PC assembly board to both the to the keyboard encoder (to lock out manual input) and to the display controller (to display the BCD control values). All of the modes, frequencies, and amplitudes are available here. If a BCD input is applied to the instrument from an external source, the manual control input is locked out.

Front Panel PC Assembly

The front panel PC assembly provides the necessary control interfacing between the front panel keyboard and the synthesizer, the external BCD input and the synthesizer, and the external GPIB input (if installed) and the synthesizer. All of these manual and external command inputs are processed on this board and converted into the necessary format to control the synthesizer and the other control modules and boards.

Z-80 Board (5155A Only)

The Z80 board, which is the heart of all the digital control circuitry, receives a clock (timing) signal that originates from the SGA board. When the unit is first turned on, the microprocessor is disabled to prevent transferring erroneous data, then initiates a routine to set up the instrument parameters.

Interrupts are received from the keyboard, BCD and GPIB boards, or when the synthesizer is loaded with a new frequency. If any interrupt is enabled, the microprocessor will read the interrupt status to locate the interrupt source, then process the information and run the various instrument routines. In BCD mode, the microprocessor is a slave to the BCD bus, being able only to read the new frequency and run the display.

GPIB (IEEE-488, Option 006) Paddle Board

The GPIB paddle board assembly meets all the handshaking requirements of the 1978 IEEE-488 standard. It handles interface protocol functions on the General Purpose Interface Bus (GPIB). A DIP switch, accessible at the rear panel, is located on this board and selects the GPIB address for the instrument.

4.3.2 Model 5156A Front Panel/Control Circuits

The remote front panel/control circuits for the 5156A consist of the front panel PC assembly and a BCD amplifier board. If the GPIB option is specified, a GPIB board and GPIB paddle board assembly will replace the BCD board.

Front Panel PC Assembly

The front panel PC assembly provides the necessary control interfacing between the synthesizer, the external GPIB input (if installed) and the external BCD input. It processes all of the external commands, converting them into the proper format to control the instrument modules and boards.

At initial power up, the IEEE controller is prevented from sending data to the unit until the IEEE control circuitry is cleared to a known state. When the IEEE controller does send frequency data, the first character sent causes the front panel PC assembly to clear any previously held frequency data. At the end of the data string, the input shift registers are returned to parallel (BCD) mode.

To insure a clean frequency transition, all IEEE or BCD frequency data is sent to the synthesizer simultaneoulsy.

An output voltage (NOTCH TUNING VOLTAGE) determined by the programmed frequency drives a notch filter located in the 500 MHz amplifier/filter RF circuit.

The BCD Amplifier Board

The BCD amplifier board converts data on the BCD bus to a voltage capable of driving the output attenuator in the RF section of the unit. BCD amplitude data is loaded and converted to binary. Output current is converted to voltage, inverted, and output.

During initial power up, the reset circuit brings the output to fullscale. The output voltage will go full scale if the rear panel BCD amplitude connector is open when a frequency is loaded.

GPIB (IEEE-488, Option 6) Board and Paddle Board

The IEEE-488 GPIB board detects amplitude and frequency parameters sent over the IEEE bus, converting amplitude data from either the BCD or IEEE bus to a voltage capable of driving the output attenuator in the RF section of the unit. Frequency data interfacing between the IEEE connector and the front panel board is provided. This board also compares the switch data (from the paddle board) with the address data from the IEEE bus.

When frequency data is sent from the IEEE data bus, the first charactor in the data string alerts the front panel board. A Group Execute Trigger (GET) or carriage return and line feed at the end of a frequency data string enables the frequency change. The IEEE controller is made to wait when the unit needs additional time to process this data.

Amplitude is set to fullscale during initial power up. If the BCD amplitude connector (J1) is open and the instrument is not programmed by the IEEE bus, the output voltage will go full scale when a frequency is loaded.

The IEEE paddle board interface connects the IEEE portion of the interface board to the rear panel connector and contains the address DIP switch, accessible at the rear panel, that is used to select the instrument address.

4.4 FREQUENCY GENERATOR CIRCUIT FUNCTIONAL BLOCK

The SGA module can be driven by any one of five factory installed configuration options:

Option 000	An external 5/10 MHz signal input via a rear panel connector.
Option 001	An internal high stability crystal oscillator of the "oven-type" operating at 10 MHz.
Option 002	An internal standard stability "TCXO" crystal oscillator.
Option 004	An internal very high stability crystal oscillator of the "oven-type" operating at 10 MHz.

The crystal oscillator functional circuit block can effectively be any one of the above options but only the standard stability option will be described here.

4.4.1 Standard Stability Oscillator

The standard stability crystal oscillator requires only a −12.6V input to produce a temperature stabilized 10 MHz output. This output is connected to the SGA module. Operating power is always applied to the oscillator when the Model 5155A/5156A is plugged in regardless of the position of the standby switch on the front panel.

4.4.2 Standard Generator "A"

Together the SGA and SGB modules produce eight frequencies required throughout the instrument. The SGA module alone produces frequencies of 18, 20, 22 and 33 MHz, each on separate outputs, and a "picket fence" (all harmonics of 10 MHz from 10 to 140 MHz) as a single output. All of the frequencies are developed from the 10 MHz standard stabilized oscillator input. The SGA also amplifies and filters the 10 MHz frequency and outputs it as the 10 MHz reference. One or more of these

SGB module to produce the 113 MHz frequency. All outputs from the SGA modules are constant and not subject to selection or control.

4.4.3 Standard Generator "B"

The SGB module receives both the 33 MHz output signal and the 10 to 140 MHz picket fence from the SGA module. It produces 14, 16, 112 and 113 MHz signals, each as a separate output. These frequencies are used by the DM and DMA modules. All outputs from the SGB modules are constant and not subject to selection or control.

4.4.4 10 MHz Amplifier

The 10 MHz reference output from the SGA is used in module 02-002-5467 and then applied to connector J5 (on the rear panel) for driving other external instruments or as a means of monitoring the internal reference frequency.

4.5 DIGITAL BOARD CIRCUIT FUNCTIONAL BLOCK

The DB1 and DB2 modules determine the digits for the 0.1 Hz to 10 kHz ranges. Digits for the 1 thru 10 kHz ranges are produced by the DB1 board, while those for ranges .1 through 100 Hz are produced by the DB2 board. Together, these boards control a digital-to-analog converter (DAC) located on the DB1 board.

The frequency, as programmed from either the standard front panel or the remote front panel, enters the digital boards in BCD format. The BCD format is converted to binary and stored in a frequency register. The output of the digital boards is a signal between 1 and 2 MHz (1.000 to 1.999,999,9 MHz).

4.6 UPCONVERTER FUNCTIONAL BLOCK

The upconverter module is used to translate the 1 to 1.999,999,9 MHz output from DB1 to a higher frequency of between 14 and 14.999,999,9 MHz for use as an input to the DM module.

A filter at the input of the upconverter picks off the 130 MHz signal from the 10-140 MHz picket fence signal. This frequency is divided by 10 to become a 13 MHz source. When mixed with the 1 to 1.999,999,9 MHz signal from the DB1 board, a 14 to 14.999,999,9 MHz signal is produced. For digits up to and including 10 kHz, the output frequency is 14 MHz for settings of all zeroes and is 14.999,999,9 MHz for settings of all nines.

4.7 DIGIT MODULE FUNCTIONAL BLOCK

The digit module (DM) generates the 100 kHz digit. This module is very similar to the DMA module which it feeds. As well as containing the 100 kHz steps, the DM module output (14.000 to 14.999,999,9 MHz) also contains all the finer steps down to 0.1 Hz that were developed in the digital boards.

The DM module uses frequencies from the SGA (18, 20, and 22 MHz) and SGB (14, 16, 112, and 113 MHz) modules to modify the upconverter signal (between 14.000 and 14.999,999,9 MHz).

For any 100 kHz digit selected, the DM uses either 112 MHz (for all even digits) or 113 MHz (for all odd digits) and one of the five lower frequencies, 14 MHZ for digits 0 and 1, 16 MHz for digits 2 and 3, 18 MHz for digits 4 and 5, etc.

The DM module moves each digit below the decimal point one position to the right and inserts a new digit (the 100 kHz frequency digit of the instrument) in the space provided. For example, if the DM module input signal is 14.210 MHz and the instrument 100 kHz frequency digit is 3, the output frequency of the DM module will be 14.3210 MHz. The DM output signal is used to drive the DMA module.

4.8 DIGIT MODULE "A" FUNCTIONAL BLOCK

The digit module "A" (DMA) generates the 1 MHz digit. This module is very similar to the DM module which feeds it. As well as containing the 1 MHz steps, the DMA module output (140 to 149.999,999,9 MHz) also contains all the finer steps down to 0.1 Hz.

The DMA module uses fixed bus signal frequencies from the SGA (18, 20, 22 MHz) and SGB (14, 16, 112, and 113 MHz) modules to modify the signal from the DM module (between 14 and 14.999,999,9 MHz).

For any DMA dial setting selected, the DMA module uses either 112 MHz (for all even digits) or 113 MHz (for all odd digits) and one of the five lower frequencies, 14 MHz for digits 0 and 1, 16 MHz for digits 2 and 3, 18 MHz for digits 4 and 5, etc.

In effect, the DMA module moves each digit above the decimal point one position to the left and inserts a new digit in the space provided. For example, if the DMA input signal is 14.321 MHz and the DMA dial setting is "6", the DMA output signal will be 146.321 MHz.

The DMA output signal (140 to 149.999,999,9) is used to drive the mixer in the 875 AMP/Mixer module which is part of the wide band translation circuit.

4.9 PHASE LOCK LOOP CIRCUIT FUNCTIONAL BLOCK

The Phase Lock Loop and Voltage Controlled Oscillator circuits provide the 10 and 100 MHz steps of frequency resolution. The voltage controlled oscillator output

drives the distribution amplifier module. The distribution amplifier module feeds both the picket fence mixer and the output mixer. It also returns a sample of its output signal to the input of the phase locked loop circuit to develop a correction signal if a frequency/phase error develops.

4.9.1 Phase Locked Loop

The inputs to the Phase Locked Loop (PLL) board are the 10 MHz reference from the SGA module, digital frequency control from the front panel, and a sample of the distribution amplifier output frequency.

A set of control voltages (dependent upon the desired frequency) is input from the front panel circuits along with the 10 MHz reference frequency from the SGA module. The control voltages set a programmable divider to the desired value. The programmable divider will then divide the sample frequency from the distribution amplifier module, compare the divided output to the reference frequency, and convert the frequency/phase error to a proportional dc error voltage. The error voltage is then fed to the voltage controlled oscillator module.

4.9.2 Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) has a natural frequency of between 735 and 1225 MHz. An error voltage input from the PLL will be applied to four nearly identical parallel oscillators (each one covering just a part of the 735 to 1225 MHz band). Only one of the oscillators is enabled at any one time by a control input from the front panel. The VCO output is fed directly to the distribution amplifier.

4.9.3 Distribution Amplifier

The Distribution Amplifier (DA) uses three separate amplifier/attenuation paths to amplify and isolate the 735 to 1225 MHz VCO signal since each of the circuits (picket fence mixer, output mixer, and phase lock loop circuit) fed by the distribution amplifier output requires a different signal level.

4.10 PICKET FENCE MIXER CIRCUIT FUNCTIONAL BLOCK

The Picket Fence Mixer Circuit consists of the 10 MHz harmonic generator and the picket fence mixer module. The 10 MHz harmonic generator supplies only one of the two inputs required for the picket fence mixer module.

4.10.1 10 MHz Harmonic Generator

The 10 MHz Harmonic Generator (HG) accepts the 10 MHz reference signal from the SGA module and creates a string of harmonics from 10 MHz to 350 MHz. The HG module has a diode circuit that clips the 10 MHz reference sinewave to produce a pulse rich in harmonics in addition to the original frequency.

4.10.2 Picket Fence Mixer

The Picket Fence Mixer (PF Mixer) mixes the picket fence signal from the harmonic generator with the 735 to 1225 MHz frequency from the distribution amplifier and uses the sum or difference frequency to drive the comb amplifier/filter circuit. The correct harmonic of the picket fence signal is always used so that when mixed with the distribution amplifier frequency of between 735 and 1225 MHz, the PF Mixer will have a 875 MHz sum or difference output.

4.11 COMB AMPLIFIER/FILTER CIRCUIT FUNCTIONAL BLOCK

The Comb Amplifier/Filter Circuits consist of the filter preamp assembly, filter assembly, and the filter post amplifier assembly. It passes only the 875 MHz signal as an "LO" input to the 875 mixer module.

4.11.1 Filter Preamp Assembly

The Filter Preamp (FP) Assembly contains a hybrid amplifier (IC) in a shielded metal container. It is used to amplify the PF Mixer output for use by the filter assembly.

4.11.2 Filter Assembly

The Filter (F) Assembly removes all but the 875 MHz frequency of the PF Mixer output signal as amplified by the filter preamp assembly. The filtered output drives the filter post amplifier assembly.

4.11.3 Filter Post Amplifier Assembly

The Filter Post Amplifier (FPA) Assembly contains an amplifier subassembly to increase the level of the 875 MHz output of the filter assembly before it enters the 875 MHz mixer/730 MHz BPF circuits. The same hybrid amplifier IC is used here as was used in the filter preamp assembly.

4.12 875 MHz MIXER/730 MHz BPF CIRCUIT FUNCTIONAL BLOCK

The 875 MHz mixer/730 MHz BPF circuits combine the 875 MHz portion of the picket fence mixer signal from the filter post amplifier with the DMA output signal, then removes all but the 725 to 735 MHz signal.

4.12.1 875 MHz Amplifier/Mixer Assembly

The 875 MHz signal from the comb amplifier/filter is fed to the 875 MHz amplifier/mixer. It contains amplifiers

to provide the necessary signal gain to drive a double-balanced mixer. The double-balanced mixer mixes the 875 MHz input with the 140-150 MHz input from the DMA module to produce a center frequency signal.

4.12.2 725-735 MHz BPF Assembly

The input to the 730 MHz BPF is the desired difference frequency from the 875 amplifier/mixer and also the sum and "LO" leakage signals. The 725-735 MHz BPF blocks all but the difference frequency from the 875 MHz amplifier/mixer. The output of this filter is used as one of two inputs to the output mixer module.

4.13 OUTPUT MIXER CIRCUIT FUNCTIONAL BLOCK

The Output Mixer (OM) consists of amplifiers and a double-balanced mixer. The signal from the 730 MHz BPF is amplified to the correct level for use in the mixer. The double-balanced mixer combines the 730 MHz bandpass filter output with the 735 to 1225 MHz signal from the distribution amplifier. The resulting output signal can be any frequency from 1 to 500 MHz. This signal is then input to the 500 MHz LPF circuits.

4.14 500 MHz AMPLIFIER/FILTER CIRCUIT FUNCTIONAL BLOCK

The 500 MHz Amplifier/Filter Circuit consists of 3 separate filters. Together, they amplify and filter the output mixer signal for use by the automatic gain control circuit.

4.14.1 500 MHz Low Pass Filter 1

The 500 MHz circuits in the 500 MHz Low Pass Filter 1 (500 MHz LPF1) partially block signals above 500 MHz that originate from the output mixer. This leaves the programmed frequency to enter the amplifier/500 MHz low pass filter.

4.14.2 Amplifier/500 MHz Low Pass Filter

The signal from 500 MHz low pass filter 1 enters the Amplifier/500 MHz Low Pass Filter (AMP/500 MHz LPF) and is filtered before being amplified. A tuning voltage from the front panel is added to the signal at this point to eliminate an unwanted frequency spur. The frequency of the spur varies as the programmed frequency changes. For each frequency programmed by the front panel or remote bus, the frequency of this spur has been calculated by the front panel circuitry and the correct tuning voltage is input. The signal is then amplified and output to 500 MHz Low Pass Filter 2.

4.14.3 500 MHz Low Pass Filter 2

The 500 MHz Low Pass Filter 2 (500 MHz LPF2) is identical to the 500 MHz low pass filter 1 described above. The output of this circuit, at 50Ω impedance, drives the automatic gain control circuitry.

4.15 AUTOMATIC GAIN CONTROL FUNCTIONAL BLOCK

The Automatic Gain Control (AGC) circuit prepares the 500 MHz amplifier/filter circuit output signal for use by the doubler and bandswitch circuits.

The 500 MHz amplifier/filter output signal is amplified, passed through a voltage controlled diode attenuator, and applied to a 3-way power splitter. The first two power splitter outputs fed the doubler and the bandswitch 0 and 1 circuits. The third output is used as feedback to control the diode attenuator. The actual output level is set by internal module adjustments.

4.16 FREQUENCY DOUBLER FUNCTIONAL BLOCK

The Frequency Doubler (FD) receives the 1 to 500 MHz output from the automatic gain control circuit. If the front panel programmed frequency is greater than 500 MHz, the frequency doubler is activated, producing an output frequency of twice the input frequency. If the front panel programmed frequency is less than 500 MHz, the frequency doubler is de-activated and does not produce an output.

An internal diode RF switch is controlled by the TTL input and blocks the RF signal if the frequency is less than 500 MHz. If the frequency is greater than 500 MHz it passes through to a frequency doubling IC. The output of the IC is amplified and fed through a resistive splitter to produce two identical isolated outputs.

4.17 BANDSWITCHING CIRCUIT FUNCTIONAL BLOCK

The bandswitching circuits provide a signal path for the desired frequency range to be input to the summer circuit. Each bandswitch covers a different frequency range. Bandswitch 0 and 1 is used for programmed frequencies up to 500 MHz, bandswitch 2 for frequencies between 500 MHz and 750 MHz, and bandswitch 3 for frequencies between 750 MHz and 1000 MHz.

4.17.1 Bandswitch 0 and 1

Bandswitch 0 and 1 (BDSW1) receives the 1 to 500 MHz directly from the automatic gain control circuit. It is amplified and applied directly to two diode switches. The diode switches are controlled by the TTL input from the front panel. If the programmed frequency is greater than 500 MHz the RF signal is effectively cut off. The bandswitch 0 and 1 output is one of three inputs to the summer module.

4.17.2 Bandswitch 2

The input for Bandswitch 2 (BDSW2) is the 500 to 1000 MHz output from the doubler circuit. When bandswitch 2 is "on", its output will be between 500 to 750 MHz due to the switching and filter circuit incorporated in its design. When bandswitch 2 is turned off, all frequencies are stopped. This bandswitch also incorporates a special TTL notch filter (that operates only between 500 and 560 MHz) that, when used with the TTL control input, eliminates undesirable spurs that develop at around 750 MHz. The bandswitch 2 output (via the band pass filter 3024) is the second of three inputs to the summer module.

4.17.3 Bandswitch 3

Bandswitch 3 (BDSW3) receives the same 500 to 1000 MHz output from the doubler circuit as does bandswitch 2. It is amplified and applied directly to two diode switches. The diode switches are controlled by the TTL input from the front panel. If the programmed frequency is less than 750 MHz the RF signal is effectively cut off. The output of bandswitch 3 (via the band pass filter 3023) is the third of three inputs to the summer module.

4.17.4 Band Pass Filter Assemblies

The bandpass filters (3023 and 3024) are passive, low insertion loss filters that are designed to pass a narrow band of frequencies and attenuate all others above and below the desired band. Bandpass "3023" passes all frequencies between 750 and 1000 MHz. At 500 MHz and below signals are attenuated at least 60 dB. At 1125 MHz and above signals are attenuated at least 45 dB. Bandpass "3024" passes all frequencies between 500 and 750 MHz. At 375 MHz and below signals are attenuated at least 55 dB. At 865 MHz and above signals are attenuated at least 35 dB.

4.18 SUMMER MODULE FUNCTIONAL BLOCK

The Summer Module (SM) is comprised of three nearly identical input circuits, a resistive summer, and an output buffer amplifier. Each of the input circuits accepts only one of the three bandswitch outputs and then directs it to the resistive summer. For any given frequency, only one of the three circuits will have a signal input. The output of the resistive summer is buffered and fed to the voltage controlled attenuator circuit.

4.19 ATTENUATOR/OUTPUT CIRCUITS

The attenuator/output circuit maintains the instrument output amplitude within preselected limits as determined by the output amplifier's RF detector feedback. A dc control voltage from the front panel is used to adjust the output to the desired level within the instruments output limits. This block consists of two separate modules; the voltage controlled attenuator and the output amplifier.

4.19.1 Voltage Controlled Attenuator

The Voltage Controlled Attenuator (VCA) module is made up of a PIN diode attenuator (using three diodes), a wideband amplifier, and the dc control amplifiers for the PIN diodes. The amount of attenuation provided by the VCA is directly proportional to the control voltage from the front panel. As the control voltage increases, the resistance to the RF signal increases decreasing the output level.

A sample of the output level is fed back to the voltage controlled attenuator from the output amplifier. This feedback maintains the output amplifier signal at a constant level as determined by the voltage controlled attenuator. Temperature compensation is also provided.

4.19.2 Output Amplifier

The RF signal from the voltage controlled attenuator is input to the Output Amplifier (OA). Hybrid wide-band amplifiers provide the necessary gain for the desired output level. A sample of the output signal is tapped off prior to the last amplifier, fed to a diode detector and sent back to the voltage controlled attenuator to maintain the correct output level.

4.20 POWER SUPPLY FUNCTIONAL BLOCK

The instrument power supply assembly actually consists of two separate power supplies (PS1 and PS3) with one supply (PS1) having an added pc board (PS2).

These power supplies generate all of the required instrument regulated dc voltages of +5.4V, −12.6V, +28V, and +6V, and also an unregulated dc voltage of +23V. All of the power supplies (PS1, PS2, and PS3) are isolated from the ac input by transformers.

4.20.1 Power Supply PS1

This power supply is conventional in design, using integrated circuit control and discrete component series pass elements. Two separate regulator circuits supply the regulated voltages of +5.4V and -12.6V. An unregulated +23V is also provided. Both regulators are short-circuit proof and have fold-back current limiting.

4.20.2 Power Supply PS2

This power supply is a lower power, higher voltage version of the regulators in PS1. It contains a similar series pass element used in the higher power regulators and in an integrated circuit for control. PS2 supplies the regulated voltage of +28V. The regulator is short-circuit proof and has fold-back current limiting.

4.20.3 Power Supply PS3

This power supply is also conventional in design, using integrated circuit control and discrete component series pass elements. This regulator supplies the high current regulated voltage of +6.0V. The regulator is short-circuit proof and has fold-back current limiting.

4.21 MODEL 5155A ELECTRICAL OPTIONS

4.21.1 Option 000

This option allows the application of an external 5 or 10 MHz customer supplied reference frequency as the only source of the 10 MHz reference required by the SGA and other modules as well. When other options are purchased, this option will also be part of the instrument configuration.

4.21.2 Option 001

This option provides an alternative to the "user-supplied" frequency reference of option 000. Option 001 is a high-stability frequency reference that uses a proportional oven to attain exceptional accuracy after initial warmup. This oscillator is self-contained and requires only a −12.6V dc supply voltage to produce an output. Refer to Section 24 for specifications.

4.21.3 Option 002

This option provides a second, less expensive and less accurate, alternative to frequency reference option 001. Option 002 is a temperature-compensated (TCXO) frequency reference that uses selected components to compensate for frequency changes due to temperature changes. This oscillator is also self-contained and requires only a −12.6V dc supply voltage to produce an output. Refer to Section 24 for specifications.

4.21.4 Option 003

This option provides the user with the ability to obtain the instrument output signal from the rear panel instead of the front panel. A rigid coax routes the rf output from the output amplifier mounted on the main chassis to the rear panel rather than to the front panel.

4.21.5 Option 004

This option provides a more accurate alternative to the frequency reference option 001. Option 004 is a very high-stability frequency reference that uses a proportional oven to attain exceptional accuracy after initial warmup. This oscillator is self-contained and requires only a −12.6V dc supply voltage to produce an output. Refer to Section 24 for specifications.

4.21.6 GPIB (IEEE-488, Option 006) for Model 5155A

This option provides the standard version (Model 5155A) with a means of communicating, as a talker or as a listener, with other instruments using the IEEE-488 bus. Both BCD and front panel operation are still available, but the interfaces are not designed to be operated simultaneously. Front panel control is locked out when BCD is in use and locked out if the local lockout is used by the IEEE.

The IEEE-488 bus commands are input to the rear panel connector that is electrically part of the IEEE-488 board itself. This board is commonly called a "paddle board" due to the construction of the board and the manner of mounting it. The IEEE-488 circuit, entirely contained on this small board, converts the standard IEEE-488 bus commands to the Model 5155A internal Z-80 command format. The Z-80 then integrates and carries out the external commands.

4.21.7 GPIB (IEEE-488, Option 006) for Model 5156A

This option provides the remote version (Model 5156A) with a means of communicating, as a listener only, with other instruments using the IEEE-488 bus. The remote feature of BCD control is still available, but the interfaces are not designed to be used simultaneously.

This option consists of two separate boards: the paddle board (9546) and the IEEE-488 board (5416). The paddle board assembly provides an interface between the external IEEE-488 bus and the internal IEEE-488 board. It also contains the IEEE-488 instrument address DIP switch which is accessible at the rear panel.

The IEEE-488 board provides all of the interfacing of the handshaking and data signals between the external bus and the internal control circuitry.

SECTION 5
MAINTENANCE, SYSTEM LEVEL

5.1 INTRODUCTION

Section 5 gives calibration procedures and, in case of malfunction, information to locate a defective module.

Calibration of two parameters is all that is required for periodic maintenance. One parameter is frequency accuracy of an option 001, 002 or 004 crystal oscillator. The time interval for corrections to crystal aging depends on the desired accuracy and crystal selected. See section 24 for calibration procedure. The other parameter is synthesizer output amplitude. Periodic checking may be required because of component aging. Readjustment of output amplitude is only necessary if the amplitude is out of specification. The recommended calibration interval for checking the amplitude is once each year. A calibration procedure for checking the amplitude is in the following section 5.2. The remainder of section 5 provides information which, in case of malfunction, permits identification of a defective module.

NOTE

Customer repair of the instrument should be performed only if the instrument cannot be returned for factory service.

All modules can be removed from the deck and replaced. Recommended field repairable or field replaceable assemblies are listed in tables 5-3, 5-4 and 5-5. The preferred module service is the exchange and factory-service of the defective module.

5.2 AMPLITUDE CALIBRATION

5.2.1 Recommended Equipment

Test equipment recommended for amplitude calibration:

Equipment	Recommended Manufacturer and Model
Microwatt Meter	Boonton 4200
Sensor	Boonton 4200-50E

5.2.2 Model 5155A Amplitude Calibration Procedure

NOTE

The completion of this procedure returns the instrument amplitude to correct alignment. ***CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS.*** *Amplitude specifications are given in section 1 of this manual.*

1. Connect the sensor between the synthesizer 50Ω connector (or rear panel SYNTH OUT if option 003 is installed) and the microwatt meter input.
2. Set the synthesizer frequency to 100 MHz.
3. Set the synthesizer amplitude to 3.1 dBm.
4. Refer to front panel board drawing 02-004-5423 (located in section 6) and adjust R14 for a reading of 3.1 ± 0.1 dBm.
5. Set the synthesizer amplitude to 13 dBm.
6. Refer to front panel board drawing 02-004-5423 and adjust R15 for a reading of 13 ± 0.1 dBm.
7. Repeat steps 3 through 6 as needed to obtain the proper results.

5.2.3 Model 5156A Amplitude Calibration Procedure

NOTE

The completion of this procedure returns the instrument amplitude to correct alignment. ***CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS.*** *Amplitude specifications are given in section 1 of this manual.*

1. Connect the sensor between the synthesizer rear panel SYNTH OUT connector and the microwatt meter input.
2. Program the synthesizer frequency to 100 MHz.
3. Program the synthesizer amplitude to 3.1 dBm.
4. Refer to front panel board drawing 02-004-5417 (located in section 6) and adjust R9 for a reading of 3.1 ± 0.1 dBm.

5. Program the synthesizer amplitude to 13 dBm.
6. Refer to front panel board drawing 02-004-5417 and adjust R10 for a reading of 13 ± 0.1 dBm.
7. Repeat steps 3 through 6 as needed to obtain the proper results.

5.3 TROUBLESHOOTING PROCEDURES

The test equipment recommended for troubleshooting is in table 5-1.

If there is no output from the instrument, proceed as follows:

1. With the instrument disconnected from the ac power source, verify the voltage selector switch on the rear panel is properly set.
2. If the instrument is equipped with an internal standard, verify that the rear panel "REFERENCE INT/EXT" switch is set to INTERNAL. Also check the rear panel "10 MHz OUT" Output connector where a 10 MHz signal (5 dBm ± 2 dB into 50Ω) should be present. If the instrument is not equipped an internal standard, set the reference to "EXT" and apply a 10 MHz ± 200 Hz + 5 dBm ± 2 dB signal to the 10 MHz reference input.
3. Remove any remote programming connectors.
4. Turn Power On. The "FRONT PANEL ACTIVE" light should come on and remain lit. If the light does not come on, check rear panel fuse. When replacing the fuse, use the proper rating as indicated on the rear panel. If the fuse is correct and the light does not come on, the bottom cover of the instrument will have to be removed.

Table 5-1. Recommended Troubleshooting Test Equipment

Equipment	Designation for Table 5-2	Required Characteristics
RF Voltmeter	"V"	1. 1 to 1.5 GHz frequency range. 2. 10 mV to 1V voltage range. 3. High impedance probe (3 pF and 100k ohms)
HF Counter	"C"	1. 0 to 1.2 GHz frequency range. 2. 10 mV sensitivity. 3. High impedance or 50 ohm input. 4. 10 Hz resolution. 5. External drive input (for synchronization with 10 MHz), 0.5V into 50 ohms or greater.
Spectrum Analyzer	"SA"	1. 0 to 1.2 GHz or greater frequency range. 2. 50 ohm input impedance. 3. 70 dB on-screen dynamic range. 4. Better than 1 kHz minimum resolution. 5. Sensitivity of −40 dBm full scale in 10 dB log display.
Multimeter	"M"	1. Analog or digital type. 2. 0 to 30V range with 0.1V resolution. 3. 0 to 2A range with 0.1A resolution.

NOTES

1. *The voltmeter and counter must have a high impedance input since connections are made to points having +5.4 Vdc present.*
2. *The RF voltmeter probe connects directly to the test points.*
3. *The counter is connected via a RG-174 or similar small diameter RF cable equipped with small alligator clips. If the input impedance is 50 Ω, make sure the test point does not have +5.4 Vdc with RF as part of the signal.*

WARNING

Disconnect the instrument power cord from the power line before removing the bottom cover. Even with the instrument power switch in the "OFF" position, standby power is still present.

5. To remove the bottom cover, remove the two screws holding the cover lip to the rear panel and carefully withdraw the cover. To fully withdraw the cover from the case, the cover has to be pressed in the middle so that the hold-down screws clear the rear panel.
6. Reconnect the power cord, turn the instrument on, and check supply voltages at the following power supply terminals:

PS1 (red wire)	+5.4V ±0.2V.
(yellow wire)	−12.6V ±0.2V.
(white wire)	+23V ±0.2V.
PS2 (green wire)	+28V ±0.2V.
PS3 (blue wire)	+6V ±0.2V.

7. If the voltages are within tolerance, then proceed to step 8. If the voltages are not within tolerance or are absent, open one output lead at a time and measure the current from the abnormal power supply. Normal currents for each of the power supplies are as follows:

   a. The +5.4V supply current should read approximately 1.5 amps.

   b. The −12.6V supply has two current paths. The first supplies standby current for the crystal oven and should read approximately 0.22 amps depending on the temperature. The second path supplies current to the synthesizer and should read approximately 0.28 amps.

   c. The +23V unregulated current from PS1 should read 0.15 amps.

   d. The +28V current from PS2 should read 0.1 amps.

   e. The +6V current from PS3 should read 1.9 amps.

8. If the signal output is still abnormal or absent, refer to table 5-2 which lists test points, signal frequencies and signal levels. These measurements are intended to isolate problems to a module level. In many cases the module inputs are digital TTL levels from the front panel interface. If the digital information is incorrect at the module inputs, then the problem is on front panel boards 5413, 5420 or 5423 on Model 5155A, or boards 5416, 5417 or 5422 on Model 5156A. Instrument designations are shown in table 5-1. Test point designations show the module type and the pin number of the board edge connector as shown on the module schematic. Figure 5-1 is a top view of the instrument showing the location of all modules and mainframe assemblies.

When proceeding from the crystal oscillator through the "frequency generator" circuits (SGA and SGB) and the "control frequency" circuits (DB1, DB2, UC, DM, and DMA), most of the tests are for the presence of a signal and/or proper frequency and can be made without opening connections. The voltmeter and counter must have a high impedance input since connections can be made to points that have 5.4 Vdc present.

To check signals from the 10 MHz harmonic generator module through to the output amplifier, 50Ω terminated SMA connections will have to be used to ensure proper circuit loading and signal measurement.

Table 5-2. Troubleshooting Chart

Test Points	Frequency (MHz)	Nominal Level (RMS)	Test Equipment Required	Module Checked
SGA, 51	10.000	0.4V	V, C	Module Input
SGA, 49	10.000	0.4V	V, C	SGA
SGA, 45	10-140	−17 dBm	SA	SGA
SGA, 43	20.000	0.1V	V, C	SGA
SGA, 20	18.000	0.1V	V, C	SGA
SGA, 6	22.000	0.1V	V, C	SGA
SGA, 2	33.000	70 mV	V, C	SGA
SGB, 20	10-140	−17 dBm	SA	Module Input
SGB, 47	33.000	70 mV	V, C	Module Input
SGB, 1	112.000	0.15V	V, C	SGB
SGB, 10	14.000	0.1V	V, C	SGB
SGB, 24	16.000	0.1V	V, C	SGB
SGB, 42	113.000	0.15V	V, C	SGB
HG, J27	10.000	0.4V	V, C	Module Input
HG, J28	10-350	−18 to −22 dBm	SA	HG
PFM, J34	10-350	−18 to −22 dBm	SA	Module Input
PFM, J33	735-1225	−3 to 0 dBm	SA	Module Input
PFM, J35	875	−34 to −38 dBm	SA	PFM
FP, J35	875	−34 to −38 dBm	SA	Module Input
FP, J39	875	−25 to −29 dBm	SA	FP
875 BPF, J39	875	−25 to −29 dBm	SA	Module Input SMA C
875 BPF, J29	875	−31 to −35 dBm	SA	FP
FPA, J29	875	−31 to −35 dBm	SA	Module Input
FPA, J30	875	−22 to −26 dBm	SA	FPA
875 AM, J30	875	−22 to −26 dBm	SA	Module Input
875 AM, J31	140-150	+2 to +5 dBm	SA	Module Input
875 AM, J32	725-735	−8 dBm	SA	875 AM
729 BPF, J32	725-735	−8 dBm	SA	Module Input
729 BPF, J37	725-735	−14 dBm	SA	729 BPF
OM, J37	875	−14 dBm	SA	Module Input
OM, J36	735-1225	+2 to +5 dBm	SA	Module Input
OM, J38	1-500	−27 dBm	SA	OM
500 LPF1, J38	1-500	−27 dBm	SA	Module Input
500 LPF1, J40	1-500	−28 dBm	SA	500 LPF1
500 AMP, J40	1-500	−28 dBm	SA	Module Input
500 AMP, J41	1-500	−7 dBm	SA	500 AMP
500 LPF2, J41	1-500	−7 dBm	SA	Module Input
500 LPF2, J45	1-500	−5 to −10 dBm	SA	500 LPF2

Table 5-2. Troubleshooting Chart (Continued)

Test Points	Frequency (MHz)	Nominal Level (RMS)	Test Equipment Required	Module Checked
AGC, J45	1-500	−5 to −10 dBm	SA	Module Input
AGC, J46	1-500	−3 dBm	SA	AGC
AGC, J47	1-500	−3 dBm	SA	AGC
FD, J48	1-500	−3 dBm	SA	Module Input
FD, J49	500-1000	+2 to +4 dBm	SA	D
FD, J50	500-1000	0 to +2 dBm	SA	D
BDSW 0&1, J51	1-500	−3 dBm	SA	Module Input
BDSW 0&1, J52	1-500	−12 to −14 dBm	SA	BDSW 0&1
BDSW 2, J55	500-750	+2 to +4 dBm	SA	Module Input
BDSW 2, J56	500-750	−6 to −8 dBm	SA	BDSW 2
BDSW 3, J53	750-1000	0 to +2 dBm	SA	Module Input
BDSW 3, J54	750-1000	−8 to −10 dBm	SA	BDSW 3
BPF, J56	500-750	−6 to −8 dBm	SA	Module Input
BPF	500-750	−8 to −10 dBm	SA	Module Output
BPF, J54	750-1000	−8 to −10 dBm	SA	Module Input
BPF	750-1000	−10 to −12 dBm	SA	Module Output
SM, J63	1-500	−12 to −14 dBm	SA	Module Input
SM, J64	500-750	−8 to −10 dBm	SA	Module Input
SM, J65	750-1000	−10 to −12 dBm	SA	Module Input
SM, J66	1-1000	−6 to +2 dBm	SA	SUMMER
VCA, J67	100	−6 to +2 dBm	SA	Module Input
OA, J72	100	+13 dBm	SA	OA
UC, J15	1-2	−17 dBm	V, C, SA	DB1, DB2
UC, J25	10-140		SA	Module Input
UC, 3	14-15	0.25V	V, C	UC
DM, 1	112.000	0.15V	V, C	Module Input
DM, 3	14-15	0.25V	V, C	Module Input
DM, 5		TTL BCD 1		Module Input
DM, 6		TTL BCD 2		Module Input
DM, 7		TTL BCD 4		Module Input
DM, 8		TTL BCD 8		Module Input
DM, 10	113.000	0.15V	V, C	Module Input
DM, 20	18.000	0.1V	V, C	Module Input
DM, 22	22.000	0.1V	V, C	Module Input
DM, 24	16.000	0.1V	V, C	Module Input
DM, 26	20.000	0.1V	V, C	Module Input
DM, 28	14.000	0.1V	V, C	Module Input
DM, 50	14-15	0.25V	V, C	DM Output

Table 5-2. Troubleshooting Chart (Continued)

Test Points	Frequency (MHz)	Nominal Level (RMS)	Test Equipment Required	Module Checked
DMA, 1	112.000	0.15V	V, C	Module Input
DMA, 3	14-15	0.25V	V, C	Module Input
DMA, 5		TTL BCD 1		Module Input
DMA, 6		TTL BCD 2		Module Input
DMA, 7		TTL BCD 4		Module Input
DMA, 8		TTL BCD 8		Module Input
DMA, 10	113.000	0.15V	V, C	Module Input
DMA, 20	18.000	0.1V	V, C	Module Input
DMA, 22	22.000	0.1V	V, C	Module Input
DMA, 24	16.000	0.1V	V, C	Module Input
DMA, 26	20.000	0.1V	V, C	Module Input
DMA, 28	14.000	0.1V	V, C	Module Input
DMA, 50	140-150	+2 to +5 dBm	SA	DMA Output
PLL, P26-1	10.000	0.4V	V, C	Module Input
PLL, P27-1		TTL "0" *	V	Module Input
PLL, P27-2		TTL "1"	V	Module Input
PLL, P27-3		TTL "1"	V	Module Input
PLL, P27-4		TTL "0"	V	Module Input
PLL, P27-5		TTL "1"	V	Module Input
PLL, P27-6		TTL "1"	V	Module Input
PLL, P27-7		TTL "0"	V	Module Input
PLL, P27-8		TTL "1"	V	Module Input
PLL, P27-9		TTL "0"	V	Module Input
PLL, J42	735-1225	+5 to +8 dBm	V, SA	Module Input
VCO, J43	735-1225	−5 to +5 dBm	SA	VCO Output
DA, J73	735-1225	−5 to +5 dBm	SA	Module Input
DA, J74	735-1225	+2 to +5 dBm	SA	DA Output
DA, J75	735-1225	−3 to 0 dBm	SA	DA Output
DA, J76	735-1225	+5 to +8 dBm	SA	DA Output

*Front Panel Set to 100 MHz

NOTES

1. The test equipment shown in table 5-2 is defined in table 5-1 as follows:
   "V" Designates a RF Voltmeter
   "T50" Designates an SMA connector with a 50Ω termination
   "C" Designates a HF Counter.
   "SA" Designates a Spectrum Analyzer.
   "M" Designates a Multimeter.
2. Ensure that the rear panel INT/EXT 10 MHz Input switch is set to INT.
3. Test point designations show the module type and the pin number (position) of the board edge connector, as used on the module schematic.
4. Set the Model 5155A/5156A to 100.000000 MHz.
5. Disconnect the SMA connector and connect SA in place of SO at J1. Each 10 MHz multiple from 10 to 140 MHz is to be displayed.

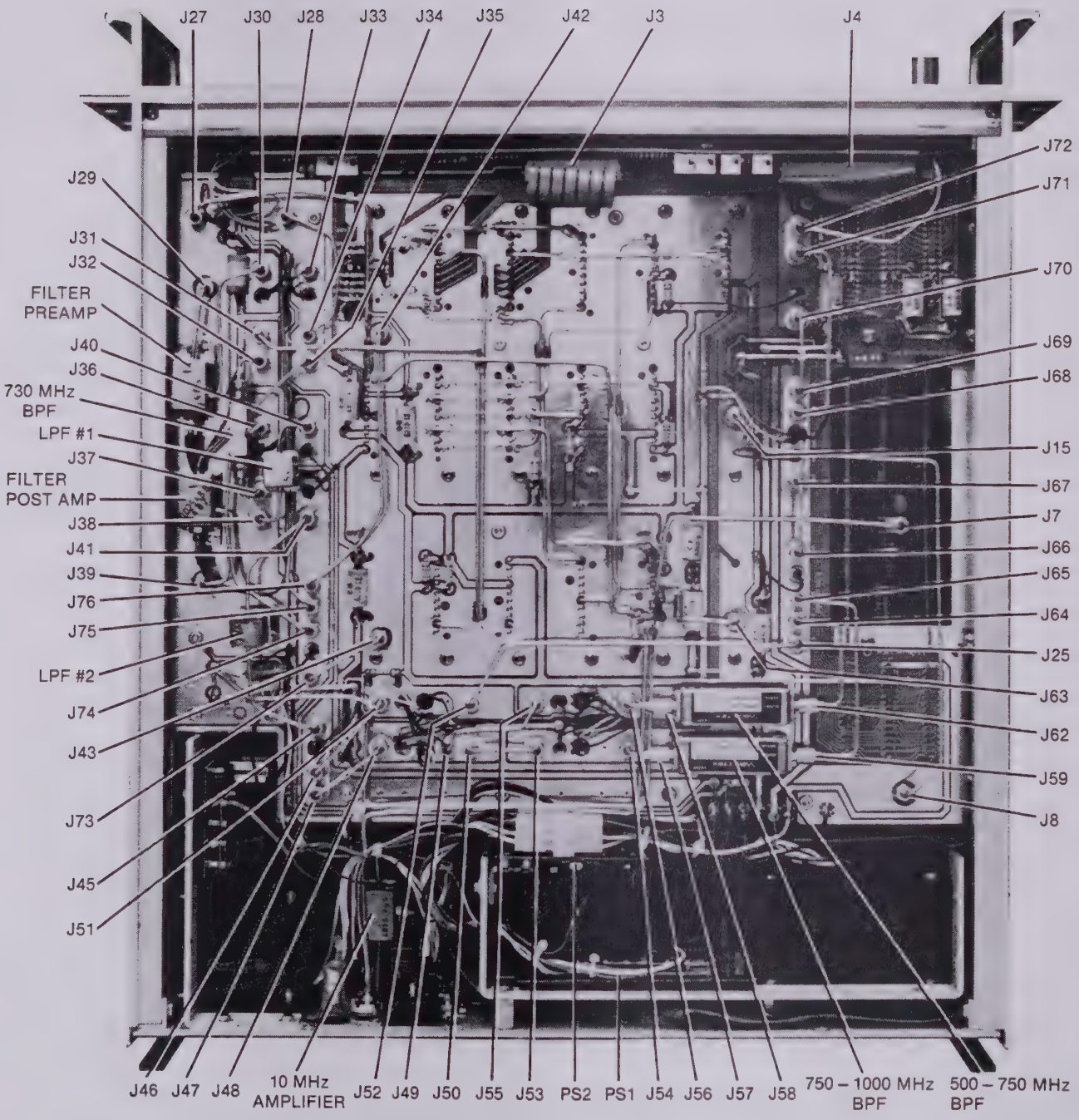


Figure 5-1. Location of Test Points

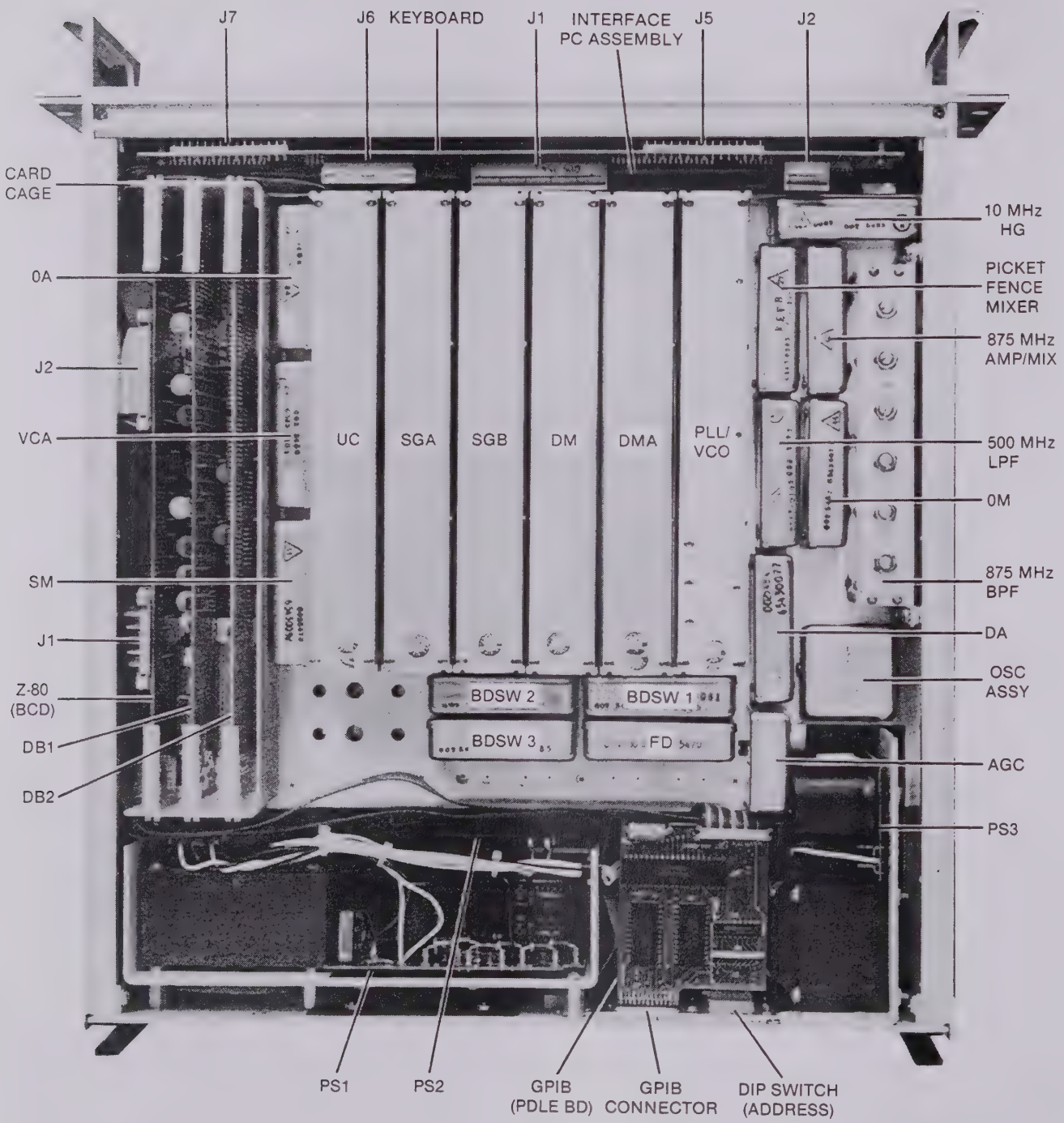


Figure 5-2. Modules and Mainframe Assemblies

Table 5-3. Field Repairable Assemblies

IEEE 488 Interface; 03-004-5414
Paddle Board; 03-004-9546

Table 5-4. Field Replaceable Assemblies

Upconverter Module; 03-004-5610
10 MHz Oscillator; 03-002-6002
10 MHz Amplifier; 03-002-5466/5467
DB1 Module; 03-004-5611
DB2 Module; 03-004-5615
DM Module; 03-004-5165
Distribution Amp; 03-004-5484
10 MHz Harmonic Generator; 03-004-5483
AMP Subassembly; 03-002-5487
Filter Post Amp; 03-004-5486
750-1000 MHz BPF; 03-004-3023
500-750 MHz BPF; 03-004-3024

Table 5-5. Assemblies Not Field Repairable or Replaceable

Keyboard; 03-004-5420
5155A Front Panel; 03-004-5423
5156A Front Panel; 03-004-5422
5156A BCD AMP; 03-004-5417
SGA Module; 03-004-5640
SGB Module; 03-004-5645
DMA Module; 03-004-5152
Phase Lock Module; 03-004-5475
VCO Module; 03-004-5478
Picket Fence-VCO Mixer; 03-004-5485
875 MHz Filter; 00-165-3021
5875 MHz AMP/Mixer Module; 03-004-5481
730 MHz BPF; 03-004-3020
Output Mixer; 03-004-5482
500 MHz LPF; 03-004-5472
Low Pass Filter #1 500 MHz; 03-002-5471
Low Pass Filter #2 500 MHz; 03-002-5474
AGC; 03-004-5480
Doubler; 03-004-5470

Table 5-5. Assemblies Not Field Repairable or Replaceable (Continued)

Bandswitch 0 & 1; 03-004-5451
Bandswitch 2; 03-004-5452
Bandswitch 3; 03-004-5453
Summer; 03-004-5473
VCA; 03-004-5459
Output Amplifier; 03-004-5460
Power Supply HCC512-501; 03-174-5013
Power Supply MAA-500; 03-174-5114
Power Supply HC5-700; 03-174-5012
Z80 Board; 03-004-5413
IEEE Board; 03-004-5416

5.4 REMOVE/INSTALL PROCEDURES

5.4.1 Instrument Cover

REMOVE

1. Position instrument right side up.
2. Remove two screws holding top cover to rear panel.
3. Remove instrument cover by sliding it to the rear.
4. Turn instrument over.
5. Remove two screws holding bottom cover to rear panel.
6. Slightly lift center of cover to allow screws holding feet to clear rear panel, then remove bottom cover by sliding it to the rear.

INSTALL

1. Position instrument right side up.
2. Insert left and right top cover edges into grooves along inside of both side panels.
3. Slide cover to front of instrument. Insure cover fits into front panel groove.
4. Fasten top cover to rear panel with two screws.
5. Turn instrument over.
6. Insert left and right bottom cover edges into grooves along inside of both side panels.
7. Slide cover to front of instrument while slightly lifting center of cover to allow screws holding feet to clear rear panel. Insure cover fits into front panel groove.
8. Fasten bottom cover to rear panel with two screws.

5.4.2 Upconverter Module

REMOVE

1. Remove instrument covers (see INSTRUMENT COVER procedure).
2. Position instrument on either side.
3. Disconnect SMA connectors J15 and J25 using a 5/8 inch open end wrench.
4. Remove three screws and lockwashers holding upconverter to chassis.
5. Carefully remove upconverter from edge connector.

INSTALL

1. Position instrument on either side.
2. Insert upconverter board edge into chassis mounted connector.
3. Fasten upconverter to chassis using three screws and lockwashers.
4. Carefully insert center conductors of semi-rigid wiring into J15 and J25 SMA connectors.
5. Hand tighten both connectors.

CAUTION

In the following step, do not over tighten SMA connectors.

6. Bring SMA connectors snug using a 5/8 inch open end wrench.
7. Install instrument covers (see INSTRUMENT COVER procedure).

5.4.3 10 MHz Oscillator (6002)

REMOVE

1. Remove instrument covers (see INSTRUMENT COVER procedure).
2. Position instrument on either side.
3. Use a ¼ inch socket wrench to remove four nuts, lockwashers and flat washers holding oscillator to chassis.
4. Unsolder five module leads from board and remove module from chassis.

INSTALL

1. Position instrument on either side.
2. Line up five module leads with holes in chassis and mount module onto board.
3. Mount and hand tighten four flat washers, lockwashers and nuts that hold oscillator to chassis.
4. Secure nuts with a ¼ inch socket wrench.
5. Solder module leads to board.
6. Install instrument covers (see INSTRUMENT COVER procedure).

5.4.4 10 MHz Amplifier (5467)

REMOVE

1. Remove instrument covers (see INSTRUMENT COVER procedure).
2. Position instrument on either side.
3. Remove blue wire connected to module by pulling it straight out.
4. Locate two semi-rigid wires passing next to SMA connectors J54 and J56, then unsolder coil and capacitor under SGA module from end of one of these wires.
5. Unsolder shielded portion of this semi-rigid wire from chassis.
6. Remove nut holding 10 MHz OUT BNC to rear panel.
7. Remove module from chassis.

INSTALL

1. Position instrument on either side.
2. Maneuver module into chassis with BNC going through rear panel 10 MHz OUT hole, and open end of semi-rigid wire positioned next to junction of coil and capacitor under SGA module.
3. Mount and secure nut holding 10 MHz OUT BNC to rear panel.
4. Solder shielded portion of semi-rigid wire to chassis.
5. Solder coil and capacitor under SGA module to end of semi-rigid wire.
6. Connect blue wire to module.
7. Install instrument covers (see INSTRUMENT COVER procedure).

5.4.5 DB1 Board

REMOVE

1. Remove instrument covers (see INSTRUMENT COVER procedure).
2. Position instrument on either side.
3. Disconnect SMA connectors J7 and J8 by using a 5/16 inch open end wrench.

4. Remove DB1 board from chassis by pulling up on extractors.

INSTALL

1. Position instrument on either side.
2. Line up DB1 board on plastic slides with components next to Z80 board and extractors pointed up.
3. Slide DB1 board into edge connectors, pushing down on extractors to secure board in place.
4. Carefully insert center conductors of semi-rigid wiring into J7 and J8 SMA connectors.
5. Hand tighten SMA connectors.

CAUTION

In the following step, do not over tighten SMA connectors.

6. Bring SMA connectors snug using a 5/8 inch open end wrench.
7. Install instrument covers (see INSTRUMENT COVER procedure).

5.4.6 DB2 Board

REMOVE

1. Remove top instrument cover only (see INSTRUMENT COVER procedure).
2. Remove DB2 board from chassis by pulling up on extractors.

INSTALL

1. Line up DB2 board on plastic slides with components next to DB1 board and extractors pointed up.
2. Slide DB1 board into edge connectors, pushing down on extractors to secure board in place.
3. Install top instrument cover (see INSTRUMENT COVER procedure).

5.4.7 DM Module

REMOVE

1. Remove instrument covers (see INSTRUMENT COVER procedure).
2. Position instrument on either side.
3. Remove three screws and lockwashers holding DM module to chassis.
4. Carefully remove DM module from three edge connectors.

INSTALL

1. Position instrument on either side.
2. Note asymmetric connector spacing, then insert DM board edge into three chassis mounted connectors.
3. Fasten DM module to chassis using three screws and lockwashers.
4. Install instrument covers (see INSTRUMENT COVER procedure).

5.4.8 Distribution Amplifier

REMOVE

1. Remove instrument covers (see INSTRUMENT COVER procedure).
2. Position instrument on either side.
3. Remove blue wire connected to module by pulling it straight out.
4. Disconnect SMA connectors J73, J74, J75 and J76 using a 5/8 inch open end wrench.
5. Remove nuts at base of SMA connectors J73, J74, J75 and J76 using a 5/8 inch socket wrench.
6. Remove module from chassis.

INSTALL

1. Position instrument on either side.
2. Line up and mount module onto chassis so that bare wire goes through largest hole.
3. Mount and hand tighten nuts on SMA connectors J73, J74, J75 and J76.
4. Secure nuts on SMA connectors using a 5/8 inch socket wrench.
5. Carefully insert center conductors of semi-rigid wiring into J73, J74, J75 and J76 SMA connectors.
6. Hand tighten SMA connectors.

CAUTION

In the following step, do not over tighten SMA connectors.

7. Bring SMA connectors snug using a 5/8 inch open end wrench.
8. Push blue wire over module bare wire.
9. Install instrument covers (see INSTRUMENT COVER procedure).

5.4.9 10 MHz Harmonic Generator (5483)

REMOVE

1. Remove instrument covers (see INSTRUMENT COVER procedure).

2. Position instrument on either side.
3. Remove blue wire connected to module by pulling it straight out.
4. Disconnect SMA connectors J27 and J28 using a 5/8 inch open end wrench.
5. Remove nuts at base of SMA connectors J27 and J28 using a 5/8 inch socket wrench.
6. Remove module from chassis.

INSTALL

1. Position instrument on either side.
2. Line up and mount module onto chassis so that bare wire goes through largest hole.
3. Mount and hand tighten nuts on SMA connectors J27 and J28.
4. Secure nuts on SMA connectors using a 5/8 inch socket wrench.
5. Carefully insert center conductors of semi-rigid wiring into J27 and J28 SMA connectors.
6. Hand tighten SMA connectors.

CAUTION

In the following step, do not over tighten SMA connectors.

7. Bring SMA connectors snug using a 5/8 inch open end wrench.
8. Push blue wire over module bare wire.
9. Install instrument covers (see INSTRUMENT COVER procedure).

5.4.10 Filter Post Amp (5487)

REMOVE

1. Remove bottom instrument cover only (see INSTRUMENT COVER procedure).
2. Position instrument up side down.
3. Remove blue wire connected to module by pulling it straight out.
4. Disconnect SMA connectors J35 and J39 using a 5/8 inch open end wrench.
5. Remove module from chassis.

INSTALL

1. Position instrument up side down.
2. Carefully insert center conductor of semi-rigid wire from "IN" to J35 SMA connector. Insert center conductor of remaining wire to J39 connector.
3. Hand tighten SMA connectors.

CAUTION

In the following step, do not over tighten SMA connectors.

4. Bring SMA connectors snug using a 5/8 inch open end wrench.
5. Push blue wire over module bare wire.
6. Install bottom instrument cover (see INSTRUMENT COVER procedure).

5.4.11 Filter Preamp (5486)

REMOVE

1. Remove bottom instrument cover only (see INSTRUMENT COVER procedure).
2. Position instrument up side down.
3. Remove blue wire connected to module by pulling it straight out.
4. Disconnect SMA connectors J29 and J30 using a 5/8 inch open end wrench.
5. Remove module from chassis.

INSTALL

1. Position instrument up side down.
2. Carefully insert center conductor of semi-rigid wire from "IN" to J29 SMA connector. Insert center conductor of remaining wire to J30 connector.
3. Hand tighten SMA connectors.

CAUTION

In the following step, do not over tighten SMA connectors.

4. Bring SMA connectors snug using a 5/8 inch open end wrench.
5. Push blue wire over module bare wire.
6. Install bottom instrument cover (see INSTRUMENT COVER procedure).

5.4.12 750-1000 MHz BPF (3023)

REMOVE

1. Remove bottom instrument cover only (see INSTRUMENT COVER procedure).
2. Position instrument up side down.

3. Secure filter with one hand while using a 5/16 inch open end wrench to disconnect SMA connectors J54 and J65 at filter.
4. Remove module from chassis.

INSTALL

1. Position instrument up side down.

NOTE

When filter is properly installed, Model/Serial decal can be read if unit is placed up side down with front panel nearest operator.

2. Carefully insert center conductor of semi-rigid wire from SMA connector J54 to right end of filter. Hand tighten connector.
3. Carefully insert center conductor of semi-rigid wire from SMA connector J65 to left end of filter. Hand tighten connector.

CAUTION

In the following step, do not over tighten SMA connectors.

4. Secure filter with one hand while using a 5/16 inch open end wrench to bring SMA connectors snug.
5. Install bottom instrument cover (see INSTRUMENT COVER procedure).

5.4.13 500-750 MHz BPF (3024)

REMOVE

1. Remove bottom instrument cover only (see INSTRUMENT COVER procedure).
2. Position instrument up side down.
3. Secure filter with one hand while using a 5/16 inch open end wrench to disconnect SMA connectors J56 and J64 at filter.
4. Remove module from chassis.

INSTALL

1. Position instrument up side down.

NOTE

When filter is properly installed, Model/Serial decal can be read if unit is placed up side down with front panel nearest operator.

2. Carefully insert center conductor of semi-rigid wire from SMA connector J56 to right end of filter. Hand tighten connector.
3. Carefully insert center conductor of semi-rigid wire from SMA connector J64 to left end of filter. Hand tighten connector.

CAUTION

In the following step, do not over tighten SMA connectors.

4. Secure filter with one hand while using a 5/16 inch open end wrench to bring SMA connectors snug.
5. Install bottom instrument cover (see INSTRUMENT COVER procedure).

5.4.14 IEEE-488 Interface (5414)

REMOVE

1. Remove top instrument cover only (see INSTRUMENT COVER procedure).
2. Disconnect J1 ribbon cable from IEEE-488 interface.
3. Remove four screws holding IEEE-488 interface mounting plate to rear panel.
4. Carefully manuever interface from rear panel assembly.

INSTALL

1. Carefully maneuver IEEE-488 interface into rear panel assembly with components facing up and mounting plate against rear panel.
2. Secure interface mounting plate to rear panel with four screws.
3. Connect J1 ribbon cable to IEEE-488 interface.
4. Install top instrument cover (see INSTRUMENT COVER procedure).

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ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
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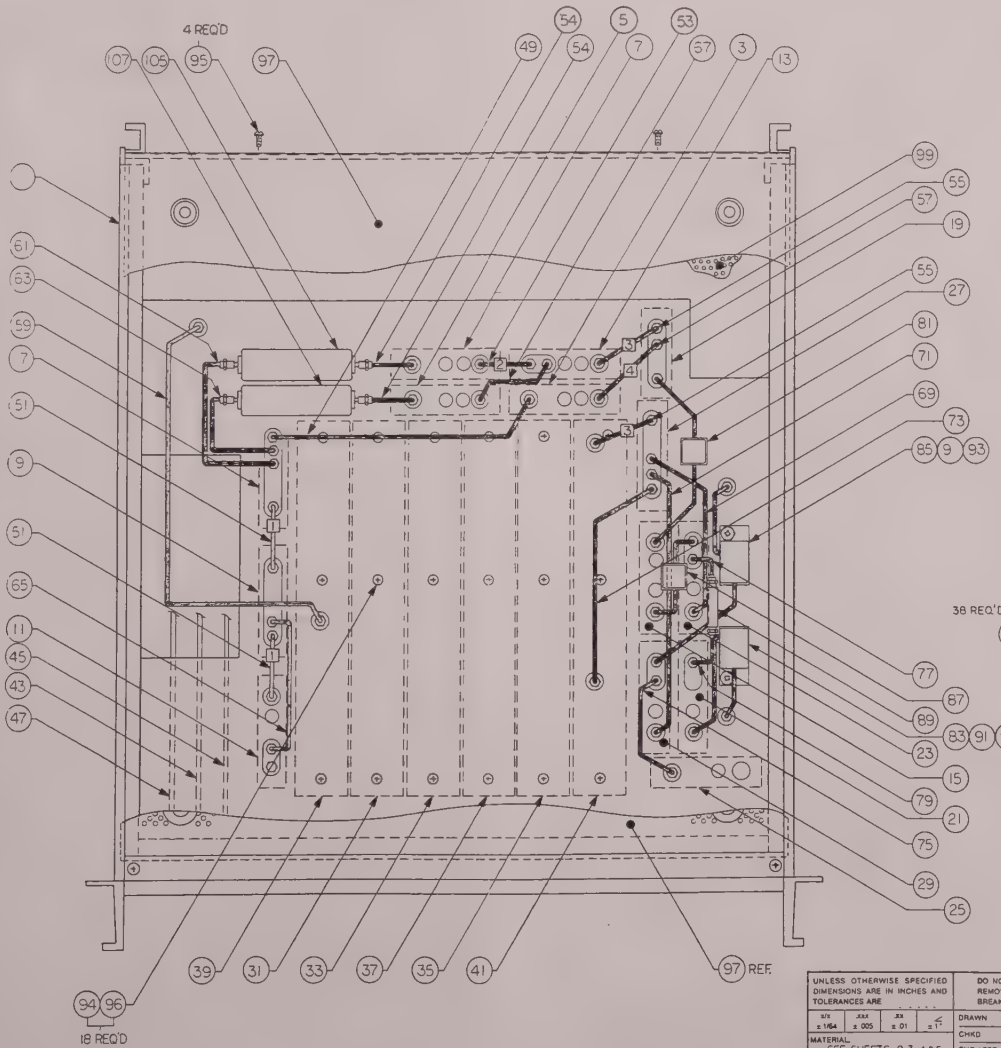

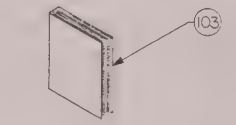

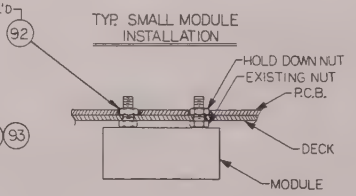

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific Inc	
.XX ± .164 .XXX ± .005 .XX ± .01 ∠ ± 1°	DRAWN JD DATE 2-16-84	TITLE	FINAL – ASSEMBLY STANDARD
MATERIAL SEE SHEETS 2,3,4 & 5 "A" SIZE	CHKD DATE 11/14/84		
FINISH	ENG APPR DATE 11/19/84	SIZE D	MODEL NO 5155 A
	MFG APPR		DRAWING NO 02-000-5400 D
	ISSUED	SCALE NONE	CODE IDENT NO 50621 SHEET 1 OF 5

WAVETEK SD INC. DWG NO. 02 000 5400 REV D

FREQ SYNTH: FINAL ASSY,STD

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	MAIN CHASSIS ASSY, 5150	002.5420	1.00
3	-	BANDSWITCH 0/1 5150	002.5451	1.00
5	-	BANDSWITCH 2, 5150	002.5452	1.00
7	-	BANDSWITCH 3, 5150	002.5453	1.00
9	-	VC ATTENUATOR MODULE, 5150	002.5459	1.00
11	-	"OA0" MODULE, 5150	002.5460	1.00
13	-	DOUBLER MODULE, 5150	002.5470	1.00
15	-	500MHZ LPF MODULE, 5150	002.5472	1.00
17	-	SUMMING MODULE, 5150	002.5473	1.00
19	-	AGC MODULE, 5150	[illegible]	1.00
21	-	874MHZ AMP/MIXER, 5150	002.5481	1.00
23	-	OUTPUT MIXER 0.1-500MHZ	002.5482	1.00
25	-	10MHZ HARMONIC GENERATOR	002.5483	1.00
27	-	BANDSWITCH #2 POSTAMP	002.5484	1.00
29	-	VCO-PF MIXER MODULE, 5150	002.5485	1.00
31	-	MODULE ASSY: 5600 "SGA"	002.5640	1.00
33	-	MODULE ASSY: 5600 "SGB"	002.5645	1.00
35	-	MODULE ASSY: 5135 DMA	002.5152	1.00
37	-	MODULE ASSY: 5120 "DM"	002.5165	1.00
39	-	MODULE ASSY: 5120 UP-CONVERTER	002.5180	1.00
41	-	PHASE-LOCK VCO MODULE, 5150	002.5475	1.00
43	-	DIGITAL BD ASSY DDS-1, 5150	004.5411	1.00
45	-	DIGITAL BD ASSY DDS-2, 5150	004.5412	1.00
47	-	Z80 PROCESSOR ASSY, 5150 STD	004.5413	1.00
49	-	CABLE ASSY: J52-J63, 5150	[illegible]	1.00
51	-	CABLE ASSY: J69-J70, 5150	009.0801	1.00
53	-	CABLE ASSY: J65-J67, 5150	[illegible]	1.00
54	-	CABLE ASSY: SEMI-RIGID 5150	009.9563	2.00
55	-	CABLE ASSY: J62-J64, 5150	009.0803	1.00
57	-	CABLE ASSY: J54-J57, 5150	[illegible]	1.00
59	-	CABLE ASSY: UC-DB1, 5150	[illegible]	1.00
61	-	CABLE ASSY: J59-J65, 5150	009.0807	1.00
63	-	CABLE ASSY: J62-J64, 5150	[illegible]	1.00
65	-	CABLE ASSY: J68-J71, 5150	[illegible]	1.00
67	-	CABLE ASSY: J49-J55, 5150	009.0810	1.00
69	-	CABLE ASSY: J36-J74, 5150	009.0811	1.00
71	-	CABLE ASSY: J33-J75, 5150	009.0815	1.00
73	-	CABLE ASSY: J42-J76, 5150	009.0820	1.00
75	-	CABLE ASSY: J28-J34, 5150	009.0821	1.00
77	-	CABLE ASSY: BPF-J37, 5150	009.0822	1.00
79	-	CABLE ASSY: BPF-J32, 5150	009.0823	1.00

WAVETEK SD INC. DWG NO. 02 000 5400 REV D

FREQ SYNTH: FINAL ASSY,STD

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
81	-	500MHZ IN-LINE LPF #2, 5150	002.5474	1.00
83	-	FILTER POSTAMP ASSY, 5150	[illegible]	1.00
[illegible]	-	FILTER PRE-AMP ASSY, 5150	002.5487	1.00
87	-	500MHZ IN-LINE LPF #1, 5150	002.5471	1.00
89	-	FILTER: BANDPASS, 729MHZ	165.3020	1.00
91	-	NUT: HEX SS 4-40 X 1/4AF	387.4001	2.00
92	-	NUT: HX BR/NI 1/4-36 X 5/16 AF	387.0143	[illegible]
93	-	WASHER: EXT LK STL CAD #4	388.1041	2.00
94	-	WASHER: SPLT LK STNLS #6	388.1062	18.00
95	-	M SCR: SS PHP 6-32 X 1/4 PH	385.6042	4.00
96	-	M SCR: SS PHP 6-32 X 3/8 PH	385.6062	18.00
97	-	BOTTOM COVER ASSY: BLK, PERF	002.5692	1.00
99	-	COVER: TOP, PERF, BLACK	304.0106	1.00
101	-	PWR CORD: 3 COND IEC, USA	378.4007	1.00
103	-	INST MANUAL: 5150 PRELIM	[illegible]	1.00
105	-	FILTER: BANDPASS, 750-1000MHZ	165.3023	1.00
107	-	FILTER: BANDPASS, 500-750MHZ	165.3024	1.00
109	NOT SHOWN	BOX: 816, 350WDW PRINTED	571.1002	1.00
111	NOT SHOWN	ETHAFOAM PIER: 6X4.5, 816-L	[illegible]	4.00
113	NOT SHOWN	ETHAFOAM PIER: 6X4.5, 816-R	585.1006	4.00

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ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
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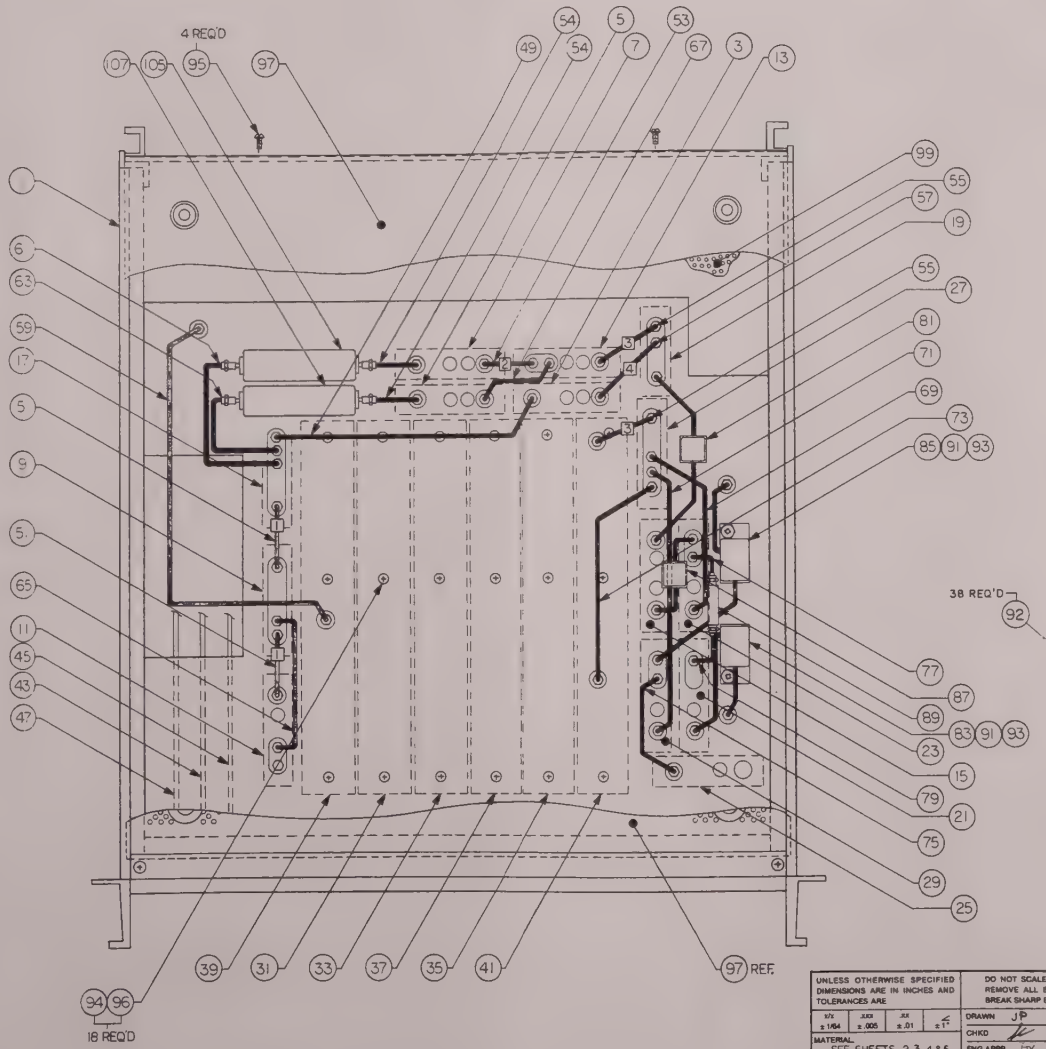
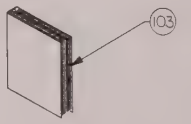
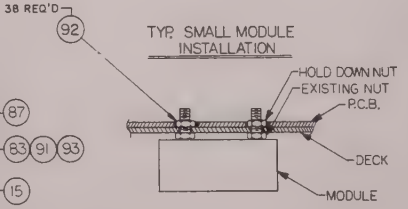
	D	9295	SH		
	E	2057	M. McMINN		11/17/16







UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific, Inc	
x/x ± 1/64 .xxx ± .005 .xx ± .01 ± 1°	DRAWN JP 3-16-84	TITLE	FINAL – ASSEMBLY REMOTE
MATERIAL SEE SHEETS 2,3,4 & 5 'A' SIZE	CHKD		
FINISH:	ENG APPR.	SIZE D	MODEL NO 5156A
	MFG. APPR.		DRAWING NO 02-000-5402
	ISSUED	SCALE NONE	CODE IDENT 50621 SHEET OF 5

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO	QUANTITY
1	-	MAIN CHASSIS ASSY, 5150 REM	002 5420	1.00
3	-	BANDSWITCH 0/1 5150	002 5451	1.00
5	-	BANDSWITCH 2, 5150	002 5452	1.00
7	-	BANDSWITCH 3, 5150	002 5453	1.00
9	-	VC ATTENUATOR MODULE, 5150	002 5459	1.00
11	-	"DAB" MODULE, 5150	002 5460	1.00
13		DOUBLER MODULE, 5150	002 5470	1.00
15	-	50MMHZ LPF MODULE, 5150	002 5472	1.00
.	-	SUMMING MODULE, 5150	002 5473	1.00
19		AGC MODULE, 5150	002 5480	1.00
21	-	870MHZ AMP/MIXER, 5150	002 5481	1.00
23	-	OUTPUT MIXER 0.1-500MHZ	002 5482	1.00
25	-	10MHZ HARMONIC GENERATOR	002 5483	1.00
27	-	BANDSWITCH #2 POSTAMP	002 5484	1.00
29	-	VCO-PF MIXER MODULE, 5150	002 5485	1.00
31	-	MODULE ASSY. 5600 "SGA"	002 5640	1.00
33	-	MODULE ASSY: 5600 "SGB"	002.5645	1.00
35	-	MODULE ASSY: 5135 DMA	002.5152	1.00
37	-	MODULE ASSY: 5120 "DM"	002.5165	1.00
39	-	MODULE ASSY: 5120 UP-CONVERTER	002.5180	1.00
41	-	PHASE-LOCK VCO MODULE, 5150	002 5475	1.00
43	-	DIGITAL BD ASSY DDS-1, 5150	004.5411	1.00
45	-	DIGITAL BD ASSY DDS-2, 5150	004.5412	1.00
47	-	BCD AMPL. CONTROL, 5150 REM	004 5417	1.00
49	-	CABLE ASSY: J52-J63, 5150	[illegible]	1.00
51	-	CABLE ASSY: J69-J70, 5150	[illegible]	2.00
53	-	CABLE ASSY: J65-J67, 5150	[illegible]	1.00
54	-	CABLE ASSY: SEMI-RIGID 5150	009 9563	2.00
55	-	CABLE ASSY: J62-J64, 5150	[illegible]	2.00
57	-	CABLE ASSY: J54-J57, 5150	009 8004	1.00
59	-	CABLE ASSY: UC-DB1, 5150	[illegible]	1.00
61	-	CABLE ASSY. J59-J65, 5150	[illegible]	1.00
63		CABLE ASSY: J62-J64, 5150	[illegible]	1.00
65	-	CABLE ASSY: J68-J71, 5150	[illegible]	1.00
67	-	CABLE ASSY: J49-J55, 5150	[illegible]	1.00
69	-	CABLE ASSY: J36-J74, 5150	009 8011	1.00
71	-	CABLE ASSY: J33-J75, 5150	[illegible]	1.00
73	-	CABLE ASSY: J42-J76, 5150	[illegible]	1.00
75	-	CABLE ASSY. J28-J34, 5150	[illegible]	1.00
77	-	CABLE ASSY: BPF-J37, 5150	[illegible]	1.00
79	-	CABLE ASSY: BPF-J32, 5150	[illegible]	1.00

WAVETEK SD INC DWG NO. 02 000 5402 REV E
FREQ SYNTH. FINAL ASSY,REMOTE

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO	QUANTITY
81		50MHZ IN-LINE LPF #2, 5150	002 5474	1.00
83		FILTER POSTAMP ASSY, 5150	002 5469	1.00
85		FILTER PRE-AMP ASSY, 5150	002 5541	1.00
87		500MHZ IN-LINE LPF #1, 5150	002 5471	1.00
89		FILTER BANDPASS, 729MHZ	155 3028	1.00
91		NUT HEX SS 4-40 X 1/4AF	321 4A0	1.00
92	-	NUT HX BRVNI 1/4-36 X 5/16 AF	321 0141	10.00
93		WASHER EXT LK STL CAD #4	388 1041	1.00
94		WASHER SPLT LK STNLS #6	388 1061	10.00
95		M SCR. SS PHP 6-32 X 1/4 PH	385 5041	4.00
96	-	M SCR: SS PHP 6-32 X 3/8 PH	385 5062	19.00
97	-	BOTTOM COVER ASSY. BLK, PERF	002 5690	1.00
99		COVER: TOP, PERF, BLACK	364 8.0E	1.00
101	-	PWR CORD- 3 COND IEC, USA	175 5007	1.00
103	-	INST MANUAL 5150 PRELIM	900 5400	1.00
105	-	FILTER BANDPASS, 750-1000MHZ	155 3021	1.00
107	-	FILTER BANDPASS, 500-750MHZ	155 3024	1.00
109	NOT SHOWN	BOX, 816, 350WDW PRINTED	571 1002	1.00
111	NOT SHOWN	ETHAFOAM PIER 6X4.5, 816-L	585 1005	1.00
113	NOT SHOWN	ETHAFOAM PIER 6X4.5, 816-R	585 1006	4.00

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ZONE	LTR	ECO NO	CHANGED BY	APP'D BY	DATE
	E	2094	M.McMINN		3/11/86

ZONE	LTR	ECO NO	CHANGED BY	APP'D BY	DATE
	A	RELEASE			
	B	2316	D		
	C	1933	S.R.		2/1/85
	D	2059	R.S.S.		11/19/85

PLL DM DMA SGB SGA

FRONT PANEL

J25 J26 J24 J23 J22 J21 J14 J13 J12 J11 J4 J3 J2 J1 J5 J9 J16 J18 J19 J17 J6

J60 J61

SMALL SHIELDED MODULE POWER & SIGNAL CHART

MODULE	+6V	+24	+28V	OTHER
5451	—	YES	—	C.L.
5452	YES	YES	—	C.L.
5453	YES	YES	—	C.L., 1750MHZ N.L.
5459	—	YES	YES	A.C.L.
5460	YES	—	—	
5470	—	YES	—	C.L.
5472	YES	—	—	T.V.
5473	YES	—	—	
5480	YES	YES	YES	
5481	YES	—	—	
5482	YES	—	—	
5483	YES	—	—	
5484	YES	—	—	
5485	YES	—	—	

NOTES:
1. ALL DIODES ARE BA244
2. LAST DESIGNATIONS R-9 C-26 CR-16 L-32
3. ALL CAPS ARE IN PF UNLESS NOTED OTHERWISE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

X/64 ±.1	XXX ±.005	XX ±.01	∠ ±1°

MATERIAL

FINISH

DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES

		DATE
DRAWN	JP	2-28-86
CHKD		9-17-87
ENG APPR.		9-17-87
MFG APPR.		9/17/87
ISSUED		

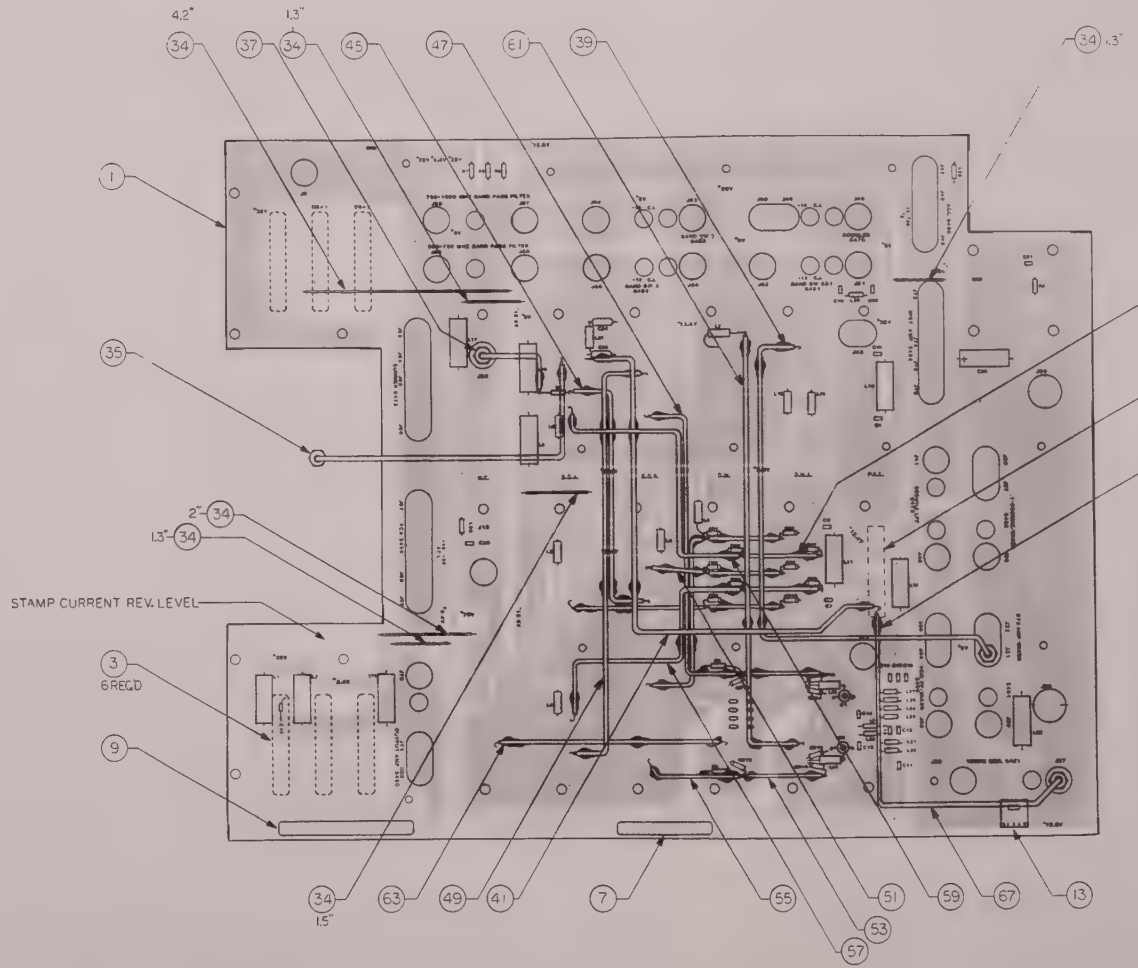
WAVETEK ROCKLAND Wavetek Rockland, Inc.

TITLE: SCHEMATIC MAINBOARD

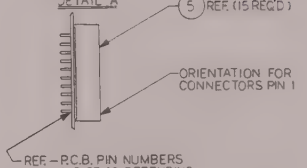
SIZE	MODEL NO	DRAWING NO	REV
D	5150	03-004-5429	E

SCALE: NONE CODE IDENT 50621 SHEET 1 OF 1

ZONE	LTR	ECO NO.	CHANGED BY	APPRD BY	DATE
	C	RELEASE			
	E	1933			
	F	2059	RSS 11-8-88		
	G				



DETAIL "A"



NOTES:
1. SEMI-RIGID CABLE SHIELDS SHOULD BE SOLDERED TO GND PLANE AS CLOSE TO CONNECTION POINT AS POSSIBLE
2. ARC SEMI-RIGID CABLES OVER ANY P.C. RUNS

DR JP	DATE	WAVETEK ROCKLAND Wavetek Rockland, Inc.
CHKD		P.C. ASSEMBLY MAINBOARD
ENG	3/2/94	
MFG	3/2/94	
ISSUED		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE		SIZE D · MODEL NO 5150 · DRAWING NO 02-004-5429 · REV G
MAT SEE SHEETS 2&3 A SIZE	FIN	SCALE 1:1 · CODE IDENT 50621 · SHEET 1 OF 3

WAVETEK SD INC. DWG NO. 02 004 5429 REV G

PC ASSY: MAINBOARD

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: MAINBOARD, 5150	320.5429	1.00
3	J6,9,16,17,18,19	CONN: PC .125 15POS DR ST	350.3001	6.00
5	J1-J5,J11-J14,J21-J26	CONN: PC .156 10POS SR ST (NE)	350.1004	15.00
7	J60	CONN: TERM 34 PIN DIL ST	354.0005	1.00
9	J61	CONN: TERM 50PIN DIL ST	354.0021	1.00
13	-	CONN: R/A PCMT 4POS JACK	354.0405	1.00
15	C24,C25,	C: FX MICA DP 560PF +-5% 500V	101.1560	2.00
16	C26,	C: FX ELECT 220UF 10V	109.7220	1.00
17	CR1 THRU CR16	CR: SWITCHING (BA482 OR BA244)	133.0244	16.00
19	R2	R: FX CFLM 150 OHM 5% 1/4W	116.1151	1.00
21	R7,R8,R9	R: FX CFLM 10K OHM 5% 1/4W	116.3101	3.00
23	R4	R: FX CFLM 470 OHM 5% 1/4W	116.1471	1.00
24	L31	L: FXD 1.0 UHY +/-10%	150.9102	1.00
25	R5,R6,	R: FX CFLM 47 OHM 5% 1/4W	116.0471	2.00
26	C3-C6,C22,C23	C: FX CER 100PF 10% X5F 500V	100.1105	6.00
27	L1-L3,L12,L15,L17,L18,L32,	L: FXD 250 UHY HI-CURR	150.1251	8.00
28	L20 THRU L30	L: FXD 10.0 UHY +/-10% MINI.	150.0101	11.00
29	L7,L13,L14	L: FXD .33 UHY +/-20%	150.8332	3.00
30	L11,L19,	L: FXD 1 MHY HI-CURR	150.2101	2.00
31	L4-L6,L8,L9,L10,L16	L: FXD 5.6 UHY +/-10%	150.9562	7.00
32	C7-C21,	C: FX CER 22PF 5% NPO 500V	100.0229	15.00
33	C1,C2,	C: VAR CER 3.5-13PF 5% 500V	108.0130	2.00
34	11.60"	WIRE: #20 AWG SOLID WHITE	378.1590	1.00
35	-	CABLE ASSY: SGA/DB1, 5150	009.0543	1.00
37	-	CABLE ASSY: SGA 10MHZ/J25	009.0544	1.00
39	-	CABLE ASSY: DMA/J31, 5150	009.0545	1.00
41	-	CABLE ASSY: PLL/SGA, 5150	009.0546	1.00
43	-	CABLE ASSY: SGBJ2/DMCR1, 5150	009.0550	1.00
45	-	CABLE ASSY: SGAJ21/SGBJ12,5150	009.0552	1.00
47	-	CABLE ASSY: SGBJ22/DMCR11,5150	009.0553	1.00
49	-	CABLE ASSY: SGAJ1/SGBJ22, 5150	009.0554	1.00
51	-	CABLE ASSY: SGBJ12/DMCR3, 5150	009.0570	1.00
53	-	CABLE ASSY: SHLD RGD FMD	009.0571	1.00
55	-	CABLE ASSY: SGBJ2/DMCR12, 5150	009.0573	1.00
57	-	CABLE ASSY: SGAJ1/DMCR4, 5150	009.0580	1.00
59	-	CABLE ASSY: SGAJ21/DMCR2, 5150	009.0581	1.00
61	-	CABLE ASSY: DMAJ3/DML7, 5150	009.0592	1.00
63	-	CABLE ASSY: UCJ5/DMJ4, 5150	009.0593	1.00
65	-	CABLE ASSY: SGAJ11/DMCR5, 5150	009.0594	1.00
67	-	CABLE ASSY: PLL/J27, 5150	009.0598	1.00

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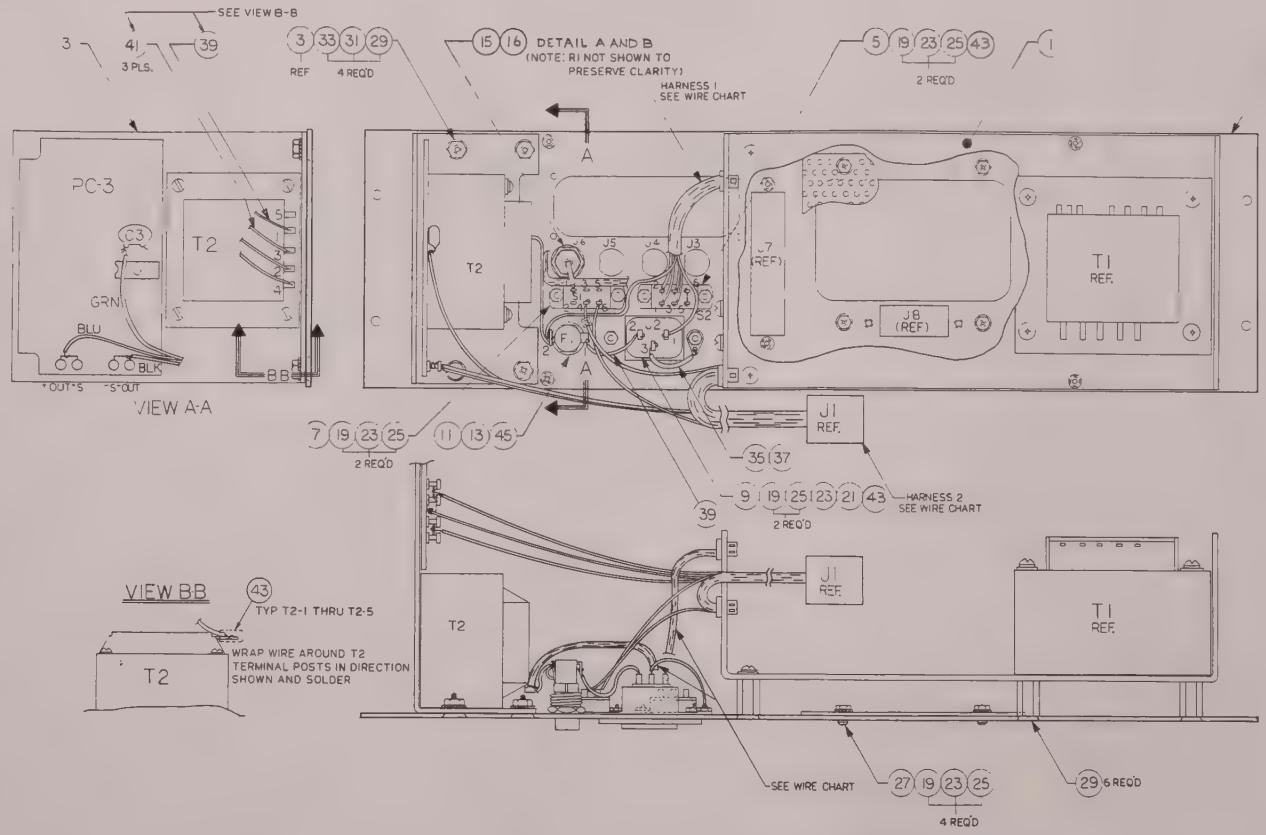
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	-702	-		
	C	2007			
	D	2093	M MCMANN		

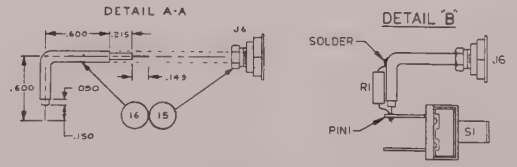


NOTE:

1. INSTALL WIRES ONTO T2 BEFORE MOUNTING ON REAR PANEL SEE VIEW B-B

WIRE CHART

BRADY MARKER	FROM	TO	COMMENTS	
1	T-4	S2-1	HARNESS #1	
2	T1-1	S2-2		
3	T.-2	S2-3		
4	T1-3	S2-4		
0 1	T1-4	J2-1		
0 2	T1-1	F1-2		
	S2-3	T2-2	20 GA. WHT.	
	S2-4	T2-3		
	J2-1	T2-4		
	F1-2	T2-1	20 GA. BLK.	
	J2-3	GND	BUSS	
	J2-2	F1-1	18 GA. BLK.	
	J6-CNTR	S1-1	BUSS	
3	S1-4	T1-*S	22 GA. YEL.	HARNESS #2
	S.-6	J1-P5	22 GA. YEL.	HARNESS #2
	PC3-OUT	J1-P4	18 GA. BLU.	
	PC3-OUT	J1-P11	BLK.	
	PC3-ut-P13	J1-P7	GRN.	
	S2-P6	S2-P5	BUSS	



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: XX ± 1/64, XXX ± .005, XXX ± .01, ANGLES ± 1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND — Wavetek Rockland, Inc.
MATERIAL: SHEET 2&3 "A" SIZE	DRAWN: JP, DATE: 8-22-83	TITLE: ASSEMBLY REAR PANEL
FINISH:	CHKD	
	ENG APPR	
	MFG APPR	
	ISSUED	
	SIZE: D, MODEL NO: 5150 A, DRAWING NO: 02-002-5495, REV: D	
	SCALE: 1:1, CODE IDENT: 50621, SHEET 1 OF 2	

WAVETEK SD INC. DWG NO. 02 002 5495 REV D

PANEL ASSY: REAR (5155A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	POWER SUPPLY ASSY, +5-12+28	002.5490	1.00
2	-	PANEL: REAR 5150	304.0608	1.00
3	-	POWER SUPPLY: 5150 +6V TESTED	174.5012	1.00
5	S2	S: SLIDE DPDT (115/230)	342.2201	1.00
7	S1	S: SLIDE DPDT	342.2200	1.00
9	J2	CONN: POWER RECEPTACLE 5600	351.0303	1.00
11	XF1	FUSE HOLDER: MINI 3 AG	351.9951	1.00
13	F1,	FUSE: 3AG 3A SB 250V	165.4014	1.00
15	J6	CONN: BNC BLKHD, RIGID COAX	351.0025	1.00
16	6"	CABLE: COAX RIGID .086DIA	378.4605	1.00
19	-	M SCR: ST CD PH 4-40 X 3/8 PH	381.4062	10.00
21	-	LUG: SOLDER FLAT #4LKG 23/32L	359.0012	1.00
23	-	WASHER: EXT LK STL CAD #4	388.1041	10.00
25	-	NUT: HX ST CD 4-40 X 1/4AF	387.4080	10.00
27	-	VENT PLATE: 5120	304.0917	1.00
29	-	SKT CSCR: BLK 8-32X3/8 82FH	386.8061	10.00
31	-	WASHER: EXT LK STL CAD #8	388.1081	4.00
33	-	NUT: HX ST CD 8-32 X 1/4AF	387.8080	4.00
35	6"	WIRE: BUSS HD DWN TND #20 AWG	378.0500	1.00
37	6"	SLVNG: TEFLON #22AWG	378.5222	1.00
39	3-1/2"	WIRE: #18 AWG STR BLACK	378.1404	1.00
41	7.00"	WIRE: #20 AWG SOLID WHITE	378.1590	1.00
42	4.00"	WIRE: #20 AWG STR BLACK	378.1504	1.00
43	FOR J2 PINS 1&2,S2 PINS 1-4	SHRINK TBG PLYFIN BLACK 3/16"	378.5530	0.00
45	FOR F1	SHRINK TBG PLYFIN BLACK 3/4"	378.5620	0.00
47	R1	R: FX CFLM 62 OHM 5% 1/4W	116.0621	1.00

SECTION 6
FRONT PANEL CIRCUITS

6.1 INTRODUCTION

The front panel board assembly for the Model 5155A contains the keyboard, status LEDs, and an LCD display. The keyboard provides manual control of the instrument unless it has been overridden by a remote connector. Front panel LEDs indicate the status of various functions including remote operation. The liquid crystal display indicates the programmed amplitude and frequency of the instrument.

The remote front panel board for the Model 5156A contains the circuitry used to process BCD and IEEE (option 006) frequency data. The source of remote operation (BCD or IEEE) is indicated by front panel mounted LEDs.

6.2 THEORY OF OPERATION

6.2.1 Model 5155A Front Panel Circuits

Keyboard Assembly

Refer to figure 6-1 and schematic 03-004-5420. Keyboard controller U4 directs the operation of both the front panel keyboard and LEDs. The keyboard is an XY matrix of switches. U4 pins 32 through 34 (S0 through S2) continuously clock a binary count of 0 through 7 to U5 pins 1, 2 and 3. At one end of the switch matrix, the decoded output of U5, (Y0 through Y7) sequentially strobes each line low. At the other end of the matrix, the R0 through R7 (U4 pins 1 through 8, 38 and 39) lines are all held high by internal pull-up resistors. When a key is pressed and the line for that key is strobed low, the corresponding line (one of R0 through R7) goes low, the interrupt request line (IRQ) at pin 4 is brought high, and the microprocessor on the Z80 board interrogates DB0 through DB7 (U4 pins 12 through 19). After determining which key was pressed, the IRQ line is again brought low.

If either the BCD or IEEE bus is controlling the instrument, U5 pin 4 will be brought high by the microprocessor through U8 pin 19. When this occurs, all U5 output pins (Y0 through Y7) remain high, disabling the front panel keys.

For any front panel LED to be lit, the cathode line (U2 pin 3 or 5) must be low, and the appropriate U3 output line (pins 11 through 18) must be high. As mentioned in the keyboard description, S0 through S2 continuously clock a binary count of 0 through 7. The 8 bit for this count, provided by S3, increases the count to 16. This bit, which drives U2 pin 1 and U1 pin 6, has a 50% duty cycle, toggling at 0 and 8. U2 pins 3 and 5 compliment each other, alternately bringing the LED cathodes low.

A small memory within U4 drives the eight ports (A0 through A3 and B0 through B3) that control PNP power driver U3. These amplifiers drive the appropriate output pin of U3 high. Suppose the "RF ON" LED is to be lit. S3 will be low, making U2 pin 6 high. Pin 5 and the "RF ON" LED cathode will now be low. U4 pin 30 will be high for the 8 cycles that S3 is low, forcing U3 pin 17 and the anode of the "RF ON" LED high. This lights the LED, but

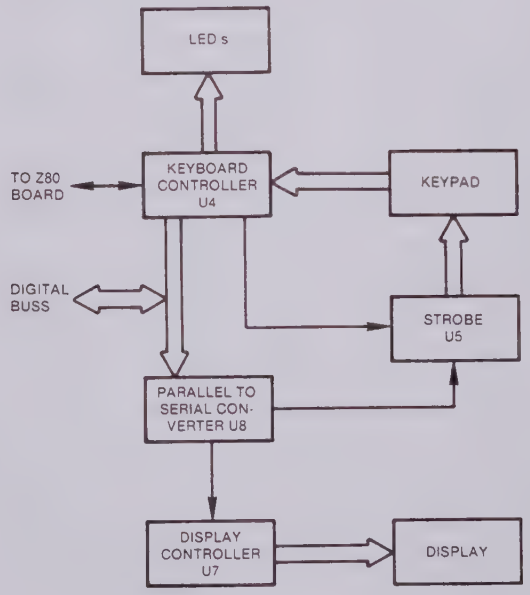


Figure 6-1. Keyboard Block Diagram

at the 50% rate described above. When U2 pin 5 returns high, the LED is extinguished. U4 pin 30 will go low unless the "LOCKED OUT" LED is also to be lit. Due to the modulation rate, the LED appears to always be lit.

The display driver (U7), controlled by U8, accepts serial information at pin 9 (SI) that is used to drive the liquid crystal display (LCD) U6. This information is either a command (with U7 pin 12 high) or data (with U7 pin 12 low) and enters U7 when clocked by the serial clock (SCK) at U7 pin 8.

U7 pins 15, 16, 17 and 19 through 49 control specific LCD segments. For any segment to be lit, it must be connected to a high and a low. Note the two digits shown in the lower right hand corner of the schematic. To light the top bar, Co must be enabled low and A must be enabled high. Each number/letter combination (1A through 10D) shown along the top and bottom edges of the LCD shown on schematic 03-004-5420 correspond to one of the 10 digits of the display. If the top bar of the fifth number is to be lit, Co must be enabled low and 10A must be enabled high. U7 continually strobes and updates the display information according to the input at pin 9. The LCD is set for optimum viewing at the factory with trim pot R10.

Interface PC Assembly

Refer to schematic 03-004-5423. Frequency or amplitude can be programmed from the front panel, IEEE interface or BCD interface. When the front panel or IEEE interface is the source of frequency programming, data travels through bidirectional parallel interface adapters U1, U2 and U3 from the "D" bus to the "PA" and "PB" bus. When the BCD interface is the source of frequency programming, data travels through U1, U2 and U3 from the "PA" and "PB" bus to the "D" bus. Decoder U20 sequentially enables U1, U2 and U3 to accept the data in either direction. U20 is enabled when control line CS and either WR or SRD are high. The appropriate interface adapter is selected by address lines A2, A3 and A4. Amplitude programming is handled in a similar manner, except that the data only travels through half of U1.

To insure clean frequency and amplitude transitions, all data is double buffered and sent to the synthesizer at the same instant. Data flows through the first buffer (U5 and U13 through U19) where each data bit is dispersed to drive multiplexers, adders or PROMS. The output of these circuits is temporarily held by a second buffer consisting of registers U41, 45, 46 and 47 on the front panel interface PC assembly and other registers located on the DB1 and DB2 boards. After the new frequency and/or amplitude parameters have been entered, an execute trigger from the programming source pulls either $\overline{\text{TRIG OUT}}$ or $\overline{\text{BCD LOAD}}$ low, clocking two single shot oscillators (U44). This simultaneously triggers registers U45 and U46, as well as other circuits on the DB1 and DB2 boards. $\overline{\text{TRIG OUT}}$ is pulled low when the programming source is either the front panel or IEEE interface. If the programming source is the BCD interface, $\overline{\text{BCD LOAD}}$ is pulled low.

PROMS U30 and U40 generate special codes for the upper two ranges (10 and 100 MHz). These codes are sent to U41 for control of the RF digit read (DR) lines, and U47 to select the proper RF bandswitch.

For frequencies up to 500 MHz, U40 pin 8 is low, causing the "A" inputs of multiplexers U22 through U29 to be inverted and placed at the "Y" outputs. Adders U32 through U39 pass data directly from their "A" inputs to their "E" outputs.

For frequencies above 500 MHz, the digital representation of the frequency value at J3 and J4 is half that of the programmed frequency input at J1. For example, if the programmed frequency is 850 MHz, the digital frequency representation at J3 and J4 will be 425 MHz. The doubler circuit in the RF section accepts a 425 MHz RF signal, outputting a frequency of 850 MHz. Above 500 MHz, PROM U40 pin 8 goes high, selecting the "B" inputs of registers U22 through U29. Note that all eight bit lines (pin 13) to these registers are held high, and all one bit lines from the programming source are input to nor gates U14 and U17 which drive the one and four bits of adders U32 through U39 on the next lower decade. U40 pin 9 is low, causing the gate outputs to compliment the one bit inputs. When any one bit is low, the nor gate output is high, adding a value of five from the "B" input at pins 6 and 15 to the "A" inputs at pins 3, 5, 12 and 14 of that adder. The least significant one bit (U12 pin 8) goes to J17 pin 28 on digital board 2, increasing the resolution from 0.1 Hz to .05 Hz so that when doubled the resolution above 500 MHz matches that of frequencies below 500 MHz.

The output pins of U41 control PROM U48 which drives digital to analog convertor (DAC) U42. The DAC current output is converted into voltage by U49 to control NOTCH TV (notch tuning voltage). The voltage on this line, which is determined by the programmed frequency, drives a notch filter located in the 500 MHz amplifier/filter RF circuit.

If frequency is programmed from J1, the rear panel 50 pin BCD interface, data is stored in tri-state registers U13, U15, U16, U18 and U19 when clocked at pin 11. At the same time, control line $\overline{\text{REMBCD}}$ from the rear panel (through J1 pin 42) goes low, sending an interrupt to the Z80 at J4 pin 4 instructing the Z80 board to place the unit in the BCD mode. With J1 pin 42 low, U12 pin 3 and therefore pin 1 of the tri-state registers are also low, enabling the BCD data to appear at the input to

multiplexers U22 through U29. As with the front panel or IEEE frequency input, the information is driven up to J3 and J4 to the synthesizer. This frequency data also travels through interface adapters U1, U2 and U3 to the "D" bus where it is sent through J6 and encoded by the Z80 to drive the display. If pin 1 of the tri-state registers (U13, U15, U16, U18 and U19) is high, the outputs are a high impedance to the connecting circuitry.

When selected by decoder U20, amplitude data programmed from the front panel or IEEE interface passes through parallel interface adapter U1 pins 2 through 9 to register U31. Control line REMBCD is high, bringing U12 pin 3 and the IC enable input at U21 pins 15 and 16 high, blocking any data from U21. The amplitude data is fed through U31 to digital to analog convertor (DAC) U50, where the digital information is changed to a current output at pin 4. U43 changes this current to a voltage of −0.25 to −3 V at ANALOG AMP which controls the VCA.

When amplitude is programmed from the BCD, data enters from J2 and passes through U5 to U21. Control line REMBCD from the rear panel 50-pin connector (J1 pin 42) goes low, bringing U12 pin 3 and the IC enable input at U5 pin 1 low. The BCD amplitude data is then allowed to pass through U21 to ANALOG AMP as previously described. This data also travels to the Z80 board through U1 and J6 in a manner similar to the frequency data.

GPIB (IEEE-488, Option 006) for Model 5155A

Refer to schematic 03-004-5414 located in section 24 of this manual. For the IEEE-488 interface, most of the protocol functions are handled by the General Purpose Interface Adapter (GPIA). This is a single IC (U1) that meets all the handshaking requirements of the 1978 IEEE-488 standard. Data and control portions of the bus require high current driving capability and specific line termination provided by bus drivers, U2 and U3. When there is a pending interrupt, $\overline{IRQ}$ (U1 pin 40) is asserted low. This alerts the microprocessor of an interrupt condition, causing it to interrogate the eight registers internal to U1. Data from the IEEE-488 bus (listen mode) is accessed by reading from the data registers in U1; data output (talk mode) is written to the same register location.

The DIP address switch, S1, selects the GPIB address for the instrument. Pull-up resistors (U5) hold input lines to U4 high unless S1 pulls one or more of these lines low. The address strobe enable line ($\overline{ASE}$) from U1 can enable the output of U4, and therefore, S1. The microprocessor reads the switch by reading data lines D0 through D7 from U4.

Z-80 Board

Refer to figure 6-2 and schematic 03-004-5413. The Z80 board is the heart of all the digital control circuitry for the 5155A, but is not included in the 5156A. The major components on this board are the Z80 microprocessor (U1), EPROM (U18), RAM (U17) and address decoder (U8).

The Z80 accepts commands from the keyboard or the IEEE-488 interface (Model 5155A Option 006) through the front panel interface board, 5423, via buffers U13, U14, U15 and bidirectional buffer U16. These buffers increase the load capability of the microprocessor, which runs the various instrument routines as dictated by software programs stored in EPROM U18. The EPROM is addressed by the "A" bus (A0-A14) when selected by chip enable ($\overline{CE}$).

As operating parameters are updated, they are sent to the instrument control circuits and front panel display via data lines D0 through D7. These parameters are also stored in, then later retrieved from, the scratch pad memory, U17, when $\overline{CS}$ (chip select) is brought low. Address lines A0 through A10 determine the location of the stored information that travels on bi-directional data lines D0 through D7. To write data into RAM, the output is disabled by a high on pin 20 and a low on $\overline{WE}$ pin 21. Reading data from RAM is accomplished by leaving $\overline{WE}$ (pin 21) high and enabling the output $\overline{OE}$ by bringing pin 20 low.

The clearinghouse for most operations on the board is the address decoder, U8. This circuit decodes A10, A11, A12 and A15 to select one of seven possible addressable devices or circuits. The address decoder output lines, which are negative true at U8, enable the keyboard ($\overline{KDSCS}$) from pin 15, display ($\overline{DISPLAY\ EN}$) from pin 9, synthesizer ($\overline{TRIG\ OUT}$) from pin 10, RF output (RF ON) from pin 11, IEEE ($\overline{IEEE\ CS}$) from pin 7, first rank synthesizer loading (CS) from pin 14 and interrupt status register ($\overline{ITR\ STATUS}$) from pin 13.

Any of three sources can independently alert the synthesizer of a frequency change. These sources are the IEEE, the Z80 (originating from the front panel) and the BCD connector. If the IEEE option is installed, it can generate a group execute trigger (GET) forcing J1 pin 18, and therefore, J18 pin 4 ($\overline{TRIG\ OUT}$) low. If the frequency is changed from the front panel, the Z80 will bring U8 pin 10 low, again forcing J18 pin 4 low. The $\overline{TRIG\ OUT}$ line is connected to the front panel board. If either this, or the $\overline{BCD\ LOAD}$ line from the BCD connector is low (enabled), the synthesizer is alerted of a frequency change.

When U8 pin 11 goes low, it directs U3 to read the status of bit D0 at pin 12, the D input. If D0 is high, RF ON will also be high, turning the output on. However, if D0 is low, RF ON will be low, turning the output off.

The $\overline{\text{IEEE}}$ $\overline{\text{CS}}$ at J1 pin 4 always follows pin 7 of U8 (IEEE EN) except when both $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are high, which brings $\overline{\text{IEEE}}$ $\overline{\text{CS}}$ high.

The Z80 can be interrupted from four sources, the keyboard (IRQ), synthesizer load ($\overline{\text{EXECUTE TRIG}}$), IEEE (IRQ), and BCD (REMBCD). These interrupts enter U10 pins 1, 4, 5 and 6 where they are summed before reaching the Z80 at pin 16. If any interrupt is enabled, the microprocessor will read the interrupt status from U13 at pins 3, 5, 7 and 9 to locate the interrupt source.

If the unit is not in any remote mode and a front panel key is pressed, J2 pin 28 (IRQ), and U13 pin 17 go high. This brings U10 pin 1 low, causing an interrupt at U1 pin 16. The microprocessor checks the "D" bus lines and discovers that D0, designating the keyboard interrupt, has been brought low (by U13 pin 3). After reading the front panel keyboard, IRQ returns low, disabling the interrupt.

When the synthesizer is loaded with a new frequency, a narrow pulse on the $\overline{\text{EXECUTE TRIG}}$ line sets U4 pin 8 low and pin 9 high until the interrupt status of U13 has been read. After the microprocessor has read the interrupt status, U12 pin 3 goes high, clearing U13 and removing the interrupt from U4 pin 8.

If the IEEE requests service, the IEEE interrupt brings J1 pin 5 ($\overline{\text{IRQ}}$) low. This line is brought high again after the microprocessor reads the IEEE input.

When the unit is addressed at the 50 pin rear panel remote BCD connector, $\overline{\text{REMBCD}}$ from J18 pin 9 goes low. This puts a high at U13 pin 13, clocks U4 pin 6 low and generates an interrupt request at the microprocessor (U1 pin 16). After the microprocessor reads the $\overline{\text{REMBCD}}$ bit at D2 (U13 pin 7), it puts the unit in BCD mode and clears the interrupt request. However, unlike other interrupt sources, $\overline{\text{REMBCD}}$ stays low and the synthesizer remains in BCD mode. In this mode, the 50 pin connector is hardwired directly to the synthesizer, making it the fastest programming path. The microprocessor is now a slave to the bus, being able only to read the new frequency and run the display. If the unit is programmed faster than the microprocessor can relay the information, the display goes blank. When the programming speed slows, the display will show the last information entered. When $\overline{\text{REMBCD}}$ returns high, control of the synthesizer returns to the microprocessor.

When the unit is first turned on, the clock generator is unstable for several cycles, causing the internal state and I/O ports to be random. To prevent transferring erroneous data during this time, U1 pin 26 is held low for a minimum of 20 ms as C2 charges to a predetermined level, disabling the microprocessor.

The 1 MHz clock signal for all the digital circuitry is supplied by U9. It divides the 10 MHz ACC CLK signal at pin 1 by 10 and applies to the microprocessor, U1 pin 6. This signal originates from the DB1 board.

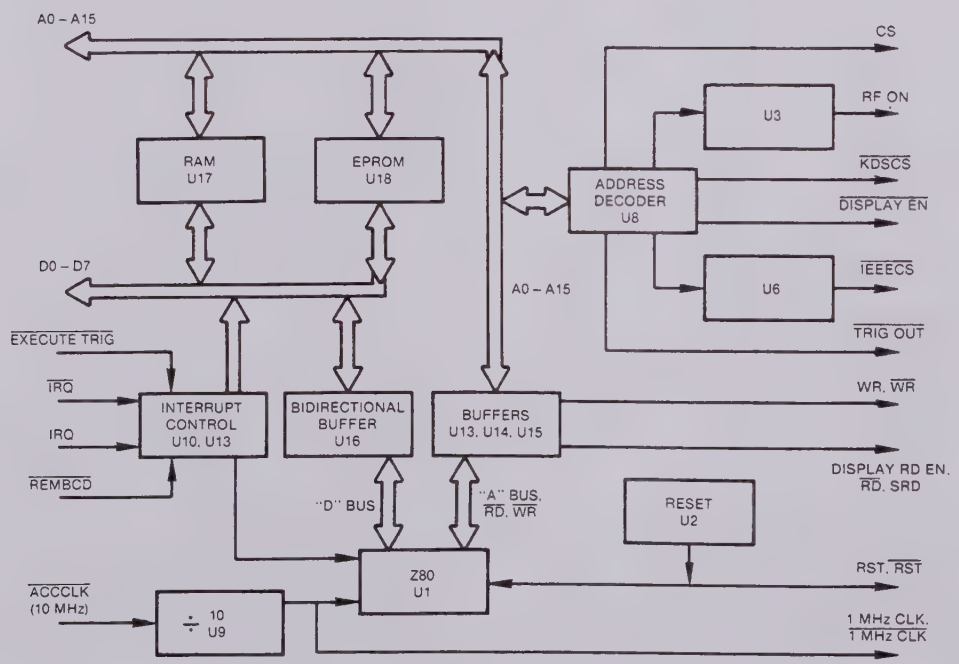


Figure 6-2. Z80 Board Block Diagram

6.2.2 Model 5156A Front Panel Circuits

Interface PC Assembly

Refer to schematic 03-004-5422. In BCD mode, parallel frequency data enters the remote front panel board through J1 and is passed to input shift registers U9, U10, U14, U15, U18, U19, U20, U21, U24 and U25 through pins 4, 5, 12 and 13. In IEEE mode, serial frequency data enters the board through J4 and is passed to the same input shift registers through pins 3, 6, 11 and 14. The logic level of U31 pin 9 determines the programming source; high for BCD, low for IEEE. Regardless of the source, this data passes through the input shift registers, traveling up the schematic to J3 and J4. From these connectors, the data enters various frequency control circuits.

At initial power up, the IEEE control circuitry shown across the bottom of the schematic is cleared to a known state. This clearing is initiated by C5 which holds U58 pin 10 low, forcing U61 pin 3 high and U61 pin 1 low. With U44 pin 2 tied high, the low at U61 pin 1 fires the U44 one-shot ($\overline{1Q}$), creating a negative going pulse at U17 pin 3. This causes U17 pin 6 ($\overline{BURST\ GATE}$) to go low, preventing the IEEE controller from sending any data to the unit.

At the same instant, U17 pin 5 goes high, enabling the clock oscillator U16, R4 and C6. Pin 10 of U31 is also pulled low by C5 during power up, forcing U31 pin 9 high, blocking any clock signal from U30 pin 8 and placing the input shift registers in parallel (BCD) mode. With U61 pin 1 low, U45 pin 6 and U13 pin 3 (1D) are both high. The clock signal is tapped at U45 pin 8 to clock U13 pin 11 and U31 pin 3.

The first clock pulse brings the high at U13 pin 3 (1D) to the 1Q output. Because the Q outputs of U13 are all connected to the next higher D inputs, each clock pulse at pin 11 brings the next Q output and D input high. When the 6Q output of U13 goes high, it also brings the 1D input of U31 high so that the next clock pulse from U45 pin 8 puts a high at U31 pin 5 (1Q). U7 pins 1 and 2 are now high, causing U7 pin 3 and U44 pin 10 to go high.

Because U44 pin 9 (2A) is tied low, pin 12 ($\overline{2Q}$) is pulsed low, clearing U13, U17, U31, U44 (1CLR) and U58, bringing all Q outputs low. U31 pin 9 (2Q) remains high because pin 13 is not cleared by U44 pin 12. With U17 pin 5 low, the U16 oscillator is now disabled and U17 pin 6 ($\overline{BURST\ GATE}$) is high, allowing the IEEE controller to begin sending data. By this time, C5 has sufficiently charged from the current through R2 to release pin 10 of U31 and U58 high. The unit is now ready to accept data over the BCD bus.

BCD data is complemented by the input shift registers and passed on to the next rank of multipliers (U26 through U29 and U32 through U35) and ROMS (U38 and U39). This data passes through adders U40 through U43 and U46 through U49 to connectors J3 and J4. To insure a clean frequency transition, all data is sent to the synthesizer when $\overline{BCD\ PROG\ LOAD}$ goes low. This enables two single shot circuits (U57), clocking $\overline{2Q}$ (pin 12) low and simultaneously triggering U52 through U55. The trigger signal also travels to other circuits as EXECUTE TRIG (J4 pins 9 and 15). PROMS U38 and U39 generate special codes for the upper two ranges (10 and 100 MHz). These codes are sent to U53 for control of the RF digit read lines, and U52 to select the proper RF bandswitch. Any new BCD data placed in the registers overwrites previous data.

If frequency data is sent from the IEEE bus, the first character, "F", is detected by the IEEE interface board (5416) which prepares the input shift registers to receive serial data from J4 by pulsing $\overline{FCLR}$ low. This in turn puils U45 pin 12 and pin 9 of all the input shift registers low. Because all BCD input lines at J1 should be high (BCD zero) a low pulse at $\overline{FCLR}$ while the input shift registers are still in parallel mode clears any previous frequency data in these registers by clocking zero into them. Dual one-shot, U62, delays the negative $\overline{FCLR}$ pulse until these registers are cleared by producing a positive pulse at U62 pin 13 followed by a negative pulse at pin 12. U31 pin 9 is cleared low and the input shift registers are ready to receive serial (IEEE) data.

For each numeral sent over the IEEE bus, U16 pin 4 ($\overline{IEEE\ DATA\ CLK}$) is pulled low. This provides a clock pulse through U45 pin 12 to shift the input register digits at U21 pins 3, 6, 11 and 14 to the left. For example, if "1234567890" is sent from the IEEE bus, the "1" will end up in U24, the "2" in U25, the "3" in U9 and so on, with "0" in U21.

When an "M" (MHz) character is sent, J4 pin 28 goes low, bringing U58 pins 11 and 9 high, and U61 pin 1 low. Because pin 1 is connected to all four IEEE data gates (U4), the shift register data inputs at U21 pins 3, 6, 11 and 14 go high, placing zero at the input of U21. With U44 pin 2 tied high, the low at U61 pin 1 fires the U44 one-shot ($\overline{1Q}$), creating a negative going pulse at U17 pin 3. $\overline{BURST\ GATE}$ goes low to prevent any additional data from being sent from the IEEE bus until the "M" has been processed. The U16 oscillator, enabled by a high at U17 pin 5, clocks pin 9 of the input shift registers through U45 pin 12. This clock signal sequentially shifts the zero at U21 to the left. The low at U61 pin 1 brings U45 pin 6 and U13 pin 3 (1D) high, which is clocked to pin 15 (Q6), bringing U31 pins 2 and 5 (1Q) high. U7 pin 3 and U30 pin 6 go high, pulsing pin 12 ($\overline{2Q}$) low. U13, U17, U31, U44 and U58 are all cleared, removing the "M" initiated from U45 pin 3 after leaving zeros in six

registers. U17 pin 5 returns low, disabling the U16 oscillator and U17 pin 6 ($\overline{\text{BURST GATE}}$) returns high, allowing the IEEE controller to again send data.

The "K" (kHz) character works in a similar manner. J4 pin 27 is brought low, bringing U58 pins 3 and 5 high. This forces U61 pin 1 low, and the sequence is duplicated as before. This time, however, the shut-off sequence begins when U13 pin 9 (4Q) goes high. This brings U6 pins 4 and 5, and U30 pins 4 and 6 all high after three zeros have entered the input shift registers through U21. The circuits are then cleared as with "M".

When a decimal point is sent, U17 pins 11 and 9 go high. This puts a premature high at U13 pin 3, starting an early count through U13 as clocked by the U16 oscillator, or $\overline{\text{IEEE DATA CLK}}$. If a decimal point and "K" are sent in the same frequency programming string, the count clears when 4Q of U13 goes high. If a decimal point and "M" are sent in the same string, the count clears when U7 pin 2 goes high.

As in BCD mode, the data string is passed on to the next rank of multiplexers, then through the adders to connectors J3 and J4. At the end of the data string, a carriage return is sent over the IEEE bus, pulling $\overline{\text{IEEE PROG LOAD}}$ flow, firing the U57 one-shots which simultaneously trigger U52 through U55 and U31 pin 11, forcing U31 pin 9 high, blocking any further clocks at U30 pin 8 and returning the input shift registers to parallel (BCD) mode.

For frequencies up to 500 MHz, U38 pin 8 is low, causing the "A" inputs (shown in U26) of multiplexers U26 through U29 and U32 through U35 to be inverted and placed at the "Y" outputs. Adders U40 through U43 and U46 through U49 pass data directly from their "A" inputs (shown in U40) to their "E" outputs.

For frequencies above 500 MHz, the digital representation of the frequency value at J3 and J4 is half that of the programmed frequency input at J1 or the IEEE programmed frequency through U4. For example, if the programmed frequency is 850 MHz, the digital frequency representation at J3 or J4 will be 425 MHz. The doubler circuit in the RF section accepts a 425 MHz RF signal, outputting a frequency of 850 MHz.

Above 500 MHz, PROM U38 pin 8 goes high, selecting the "B" inputs of multiplexers U26 through U29 and U32 through U35. Note that all one bit lines from the programming source are input to nor gates U56 and U59 which drive the one and four bits of adders U40 through U43 and U46 through U49 on the next lower decade. U38 pin 9 is low, causing the gate outputs to compliment the one bit inputs. When any one bit is low, the gate output is high, adding a value of five from the "B" input at pins 6 and 15 to the "A" inputs at pins 3, 5, 12 and 14 of that adder. The least significant one bit (U30 pin 3) goes to J17 pin 28 on digital board 2, increasing the resolution of frequencies above 500 MHz to match that of frequencies below 500 MHz.

The output pins of U53 control PROM U64 which drives digital to analog convertor (DAC) U63. The DAC current output is converted into voltage by U60 to control NOTCH TUNING VOLTAGE. The voltage on this line, which is determined by the programmed frequency, drives a notch filter located in the 500 MHz amplifier/filter RF circuit.

BCD Amplifier Control Assembly

Refer to schematic 03-004-5417. The BCD Amplifier converts data on the BCD bus to a voltage capable of driving the output attenuator in the RF section of the unit.

BCD amplitude data at J1 is loaded into U4 when AMPL CLK is brought low. U6 converts this BCD data to binary for register U9, which loads Digital to Analog Convertor (DAC) U2 when clocked at pin 11 by EXT TRIG (EXEC TRIG on front panel board 5422). Output current from U2 is converted to voltage by U1, inverted, and output at Analog Out.

During initial power up, the reset circuit (R16, CR1 and C25), brings the output of U9 to zero, forcing the output at U1 to minimum. Note that all lines between U4 and U6 are connected to pull up resistors. If J1 is not connected, the output voltage at U1 will go full scale when a frequency is loaded, clocking U9 pin 11.

GPIB (IEEE-488, Option 006) for Model 5156A

Refer to schematic 03-004-5416 located in section 24 of this manual. The IEEE interface board converts amplitude data from either the BCD or IEEE bus to a voltage capable of driving the output attenuator in the RF section of the unit. It also provides frequency data interfacing between the IEEE connector and the front panel board.

Handshaking between the IEEE bus and the IEEE interface board is provided by U14. Data interface ($\overline{\text{D1}}$ through $\overline{\text{D8}}$) is handled by U15. U16 compares the address switch data at J3 (from the paddle board) with the data from the IEEE bus. When the IEEE controller addresses this unit, the lines match, causing U16 pin 14 to bring U19 pin 22 high.

The heart of the IEEE portion of the interface board is logic array U19. In conjunction with the various logic gates and other circuitry shown in the middle and right hand portion of the schematic, this logic array detects the amplitude and frequency parameters sent over the IEEE bus. Inputs to U19 are designated "I", outputs are labeled "F". The state machine (U20) selects "unlisten",

"listen always", "amplitude", "frequency" or "e enter" modes. The selected output of the state machine can be determined by the chart at the bottom of the schematic.

Amplitude data from the BCD bus (J1) is loaded into U4 when $\overline{\text{AMPL CLK}}$ goes low, and from the IEEE bus ($\overline{\text{D1}}$ through $\overline{\text{D4}}$) into U5 when U22 pin 5 goes low. Four data lines ($\overline{\text{D1}}$ through $\overline{\text{D4}}$) are used to load the eight bit amplitude register, U5. To accomplish this, four bits are loaded at U5 pins 3, 4, 7 and 8, then clocked to output pins 2, 5, 6 and 9. This output loops back around to input pins 13, 14, 17 and 18. A second group of four bits are then entered at U5 pins 3, 4, 7 and 8. At the end of the amplitude data string, a carriage return or Group Execute Trigger (GET) clocks a low at U22 pin 5 and U5 pin 11, bringing all eight "D" input pins of U5 to the "Q" output.

Regardless of the source, BCD and IEEE programming always enters the "A" inputs of U6 as BCD data where it is converted to binary for register U9. This register loads Digital to Analog Convertor (DAC) U2 when U9 is clocked at pin 11 by EXT TRIG (EXEC TRIG on front panel board). Output current from U2 is converted to voltage by U1, inverted, and output at Analog Out. Amplitude control at U1 pin 7 (ANALOG OUT) is set to minimum during initial power up by reset circuit (R16, CR1 and C25) which brings the output of U9 to zero. Note that all lines between U4 and U6 are connected to pull up resistors. If J1 is not connected and U6 is not programmed by the IEEE bus, the output voltage at U1 will go full scale when a frequency is loaded because of the clock pulse at U9 pin 11.

When frequency data is about to be sent from the IEEE data bus, an "F" is detected which pulls U22 pins 14 and 15 low and pin 13 high. This brings $\overline{\text{IFCLR}}$ low, alerting the front panel board of frequency data coming over the data bus. Numerical data is sent over lines $\overline{\text{D1}}$ through $\overline{\text{D4}}$. These lines are inverted by U11 before reaching the front panel board. The decimal point ("$\overline{\text{DP}}$"), megahertz ("$\overline{\text{M}}$") and kilohertz ("$\overline{\text{K}}$") are decoded by U10, U12 and U13, pulling the appropriate line low. For each character sent from the IEEE bus to the front panel board, $\overline{\text{IEEE DATA CLK}}$ is brought low. A carriage return or Group Execute Trigger (GET) at the end of a frequency data string causes $\overline{\text{IEEE PROG LOAD}}$ to go low. When the unit needs additional time to process frequency data, $\overline{\text{BURST GATE}}$ from the front panel board is brought low, gating NRFD (Not Ready For Data) low.

The IEEE paddle board interface (shown in schematic 03-009-9546 located in section 24 of this manual) connects the IEEE portion of the interface board to the rear panel connector and contains the address DIP switch used to select the instrument address.

6.3 SPECIFICATIONS

6.3.1 Model 5155A Front Panel Circuits

The standard front panel circuits (boards or assemblies) have the following specifications:

Keyboard Assembly

Input Signals	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
Output Signals	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
LCD Resolution	10 digits.
LCD Controller	μPD7225.
Keyboard Controller	8279-5.
DC Supply	+5.4V at 130 mA.
Connectors	Two 15-pin terminal strips.

Front Panel PC Assembly

Input Signals	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
Input Bus	Z-80 data and control bus.
Output Signals	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
Output Bus	Z-80 data control bus.
DC Supply	+5.4V at 815 mA. +28V at 2.5 mA −12.4V at 21 mA
Connectors	Two 15-pin terminal strip. One 14-pin IDC. Two 34-pin IDC. Two 50-pin IDC.

GPIB (IEEE-488, Option 006)

Card Configuration	Paddle board construction.
Interface Controller	MC68488.
Address Control	One 8-section DIP switch.
Bus Management	Bidirectional IEEE-488 to Z-80.
DC Supply	+5.4V at 150 mA.
Connectors	One 26-pin IDC (internal). One 24-pin GPIB (external).

Z-80 Board

Microprocessor	2.0 MHz Z-80.
Start-up Memory	64 through 256 kBytes.
Operating Memory	2048 × 8 NMOS.
DC Supply	+5.4V at 300 mA.
Connectors	Two 30-pin edgecard. One 26-pin right-angle IDC. One 34-pin right-angle IDC.

6.3.2 Model 5156A Front Panel Circuits

The remote front panel circuits (boards or assemblies) have the following specifications:

Front Panel PC Assembly

Input Signals	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
DC Supply	+5.4V at 0.68 mA. +28V at 2 mA −12.4V at 14 mA
Connectors	Two 18-pin IDC. One 34-pin IDC. One 50-pin IDC.

BCD Amplifier Control Assembly

Input Signals (amp and freq)	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
Output Signals (freq)	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
DC Supply	+5.4V at 100 mA. +23V at 3 mA. −12.4V at 15 mA.
Connectors	Two 14-pin IDC. One 34-pin right-angle IDC. Two 30-pin edgecard.

GPIB (IEEE-488, Option 006)

This option consists of two separate boards. Each board is identified by the last four digits of its part number to prevent confusion with other GPIB boards.

9546 Board

Card Construction	Paddle-board.
Address Control	8-section DIP switch.
Connectors	One 26-pin IDC. One 24-pin GPIB.

5416 Board

Bus Management	Unidirectional IEEE-488 to BCD format.
Internal Signals	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
External Signals	IEEE-488 Bus.
DC Supply	+5.4V at 370 mA. −12.4V at 12 mA. +23V at 12 mA.
Connectors	One 34-pin right-angle IDC. Two 14-pin IDC. Two 30-pin edgecard.

6.4 MAINTENANCE

6.4.1 Preventive Maintenance

System level preventive maintenance is required for the front panel interface PC board. Refer to section 5.2.

6.4.2 Alignment/Calibration

See section 5.2 for the calibration of the front panel interface PC board.

Field or customer alignment of the remaining boards listed in this section is not advised. If realignment is required, return the assembly to the factory for service.

6.4.3 Troubleshooting

Chapter 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming any assembly to be faulty.

If the keyboard, Z80, IEEE, BCD amplitude or either front panel boards have been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

If the IEEE-488 interface or paddle board has been isolated as the source of the problem, use standard troubleshooting techniques to repair the board.

Replacement of faulty components on the IEEE-488 interface or paddle boards requires careful use of printed circuit repair techniques as applicable to double-sided boards with plated-through holes.

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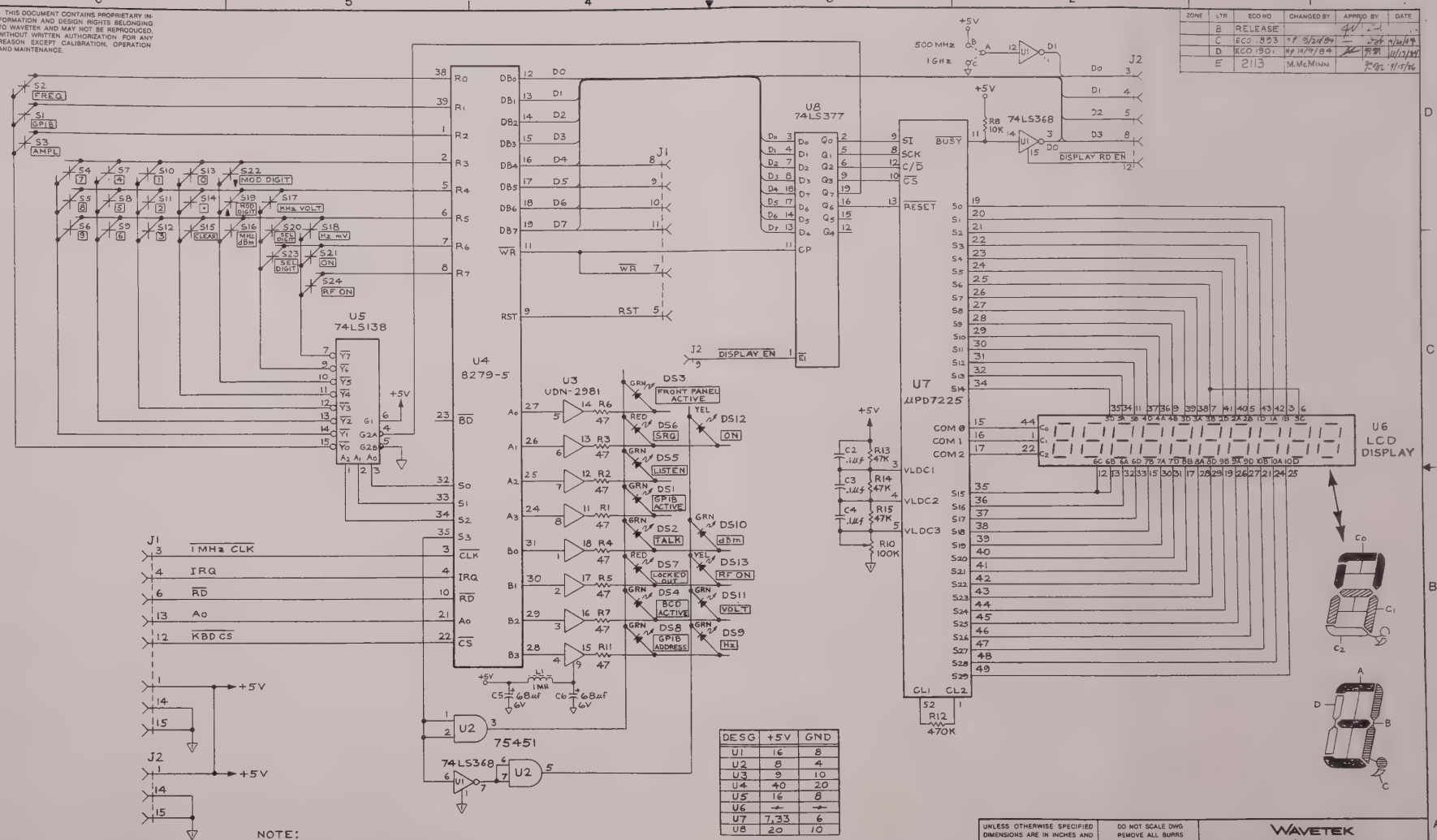
ZONE	LTR	ECO NO	CHANGED BY	APPRVD BY	DATE
	B	RELEASE			
	C	ECO 803			9/26/84
	D	ECO 901			11/13/84
	E	2113	M. McMINN		11/13/86



DESG	+5V	GND
U1	16	8
U2	8	4
U3	9	10
U4	40	20
U5	16	8
U6	—	—
U7	7,33	6
U8	20	10

NOTE:
1. ALL RESISTORS ARE IN OHM ±5%, 1/4W.

DESIGNATION NOT USED
R9, R16, C1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
x/x ±1/64 | .xxx ±.005 | .xx ±.01 | ±1°
MATERIAL:
FINISH:
DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

DRAWN 9/3/84
CHKD
ENG APPR 9/5/84
MFG APPR 9/5/84
ISSUED

WAVETEK
Wavetek Rockland Scientific Inc

TITLE: ELECTRICAL SCHEMATIC KEY BOARD STANDARD LOCAL

SIZE D | MODEL NO. 5155 | DRAWING NO. 03-004-5420 | REV E
SCALE: | CAGE CODE 50621 | SHEET 1 OF 1

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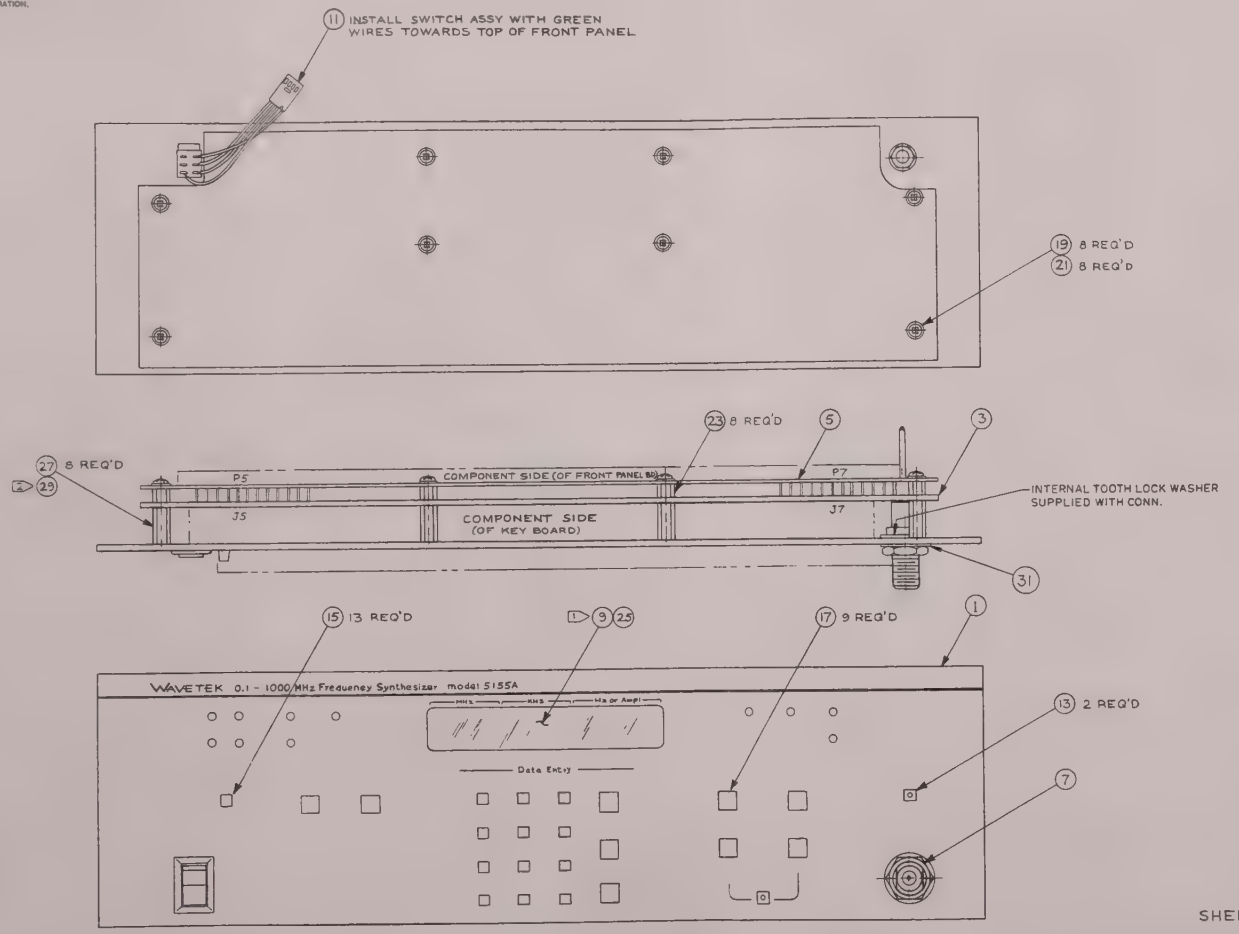
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE		RM	
	B	ECO 1901	RF 11/12/84	RM	11/13/84
	C	2064	M McMINN		



SHEET 2 IS "A" SIZE L/M

NOTE:

1. SECURE ITEM 9 TO BACK OF PANEL BY TACKING FOUR CORNERS WITH ITEM 25.
2. APPLY ITEM 29 TO THREADS OF ITEM 27.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific Inc
x/x ± 1/64 .xxx ± .005 .xx ± .01 ± 1°	DRAWN R. Peters DATE 10/5/84	TITLE: FRONT PANEL ASSY STANDARD LOCAL
MATERIAL —	CHKD [illegible] 10/8/84	
FINISH —	ENG APPR. [illegible] 10-9-84	
	MFG APPR.	
	ISSUED	SIZE D · MODEL NO 5155 · DRAWING NO 02-001-5420 · REV C
		SCALE: 1:1 · CODE IDENT 50621 · SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 001 5420 REV C

PANEL ASSY: FRONT (5155A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	FRONT PANEL: 5150 (STD)	300.5420	1.00
3	-	DISPLAY/KEYBOARD, 5150 (STD)	[illegible]	1.00
5	-	FRONT PANEL ASSY, 5150 (STD)	004.5423	1.00
7	-	CABLE ASSY: RGD COAX, J72-FP	009.0834	1.00
9	-	SHIELD: LCD DISPLAY, 5155	376.1503	1.00
11	-	CABLE ASSY: RP-FP POWER, 5150	[illegible]	1.00
13	-	KNOB: PB SQ GRY LIGHTED 5830	370.0763	2.00
15	-	KNOB: PB SQ BLK 5830	370.0764	13.00
17	-	KNOB: WHT 0-9/36 5120 BLK/MK	370.0766	9.00
19	-	M SCR: ST CD PH 6-32 X 3/8 PH	381.6062	8.00
21	-	WASHER: SPLT LK STNLS #6	388.1062	8.00
23	-	SPR: THD M/F 1/4HX 6-32X1/4	389.2034	[illegible]
25	-	ADHESIVE: PASTE, CLEAR (RTV)	500.2001	1.00
27	-	SPR: THD 1/4HX 6-32X.687	389.2016	8.00
29	-	LOCTITE #242	[illegible]	1.00
31	-	WASHER: FLAT STL CAD .636 ID	388.0631	1.00

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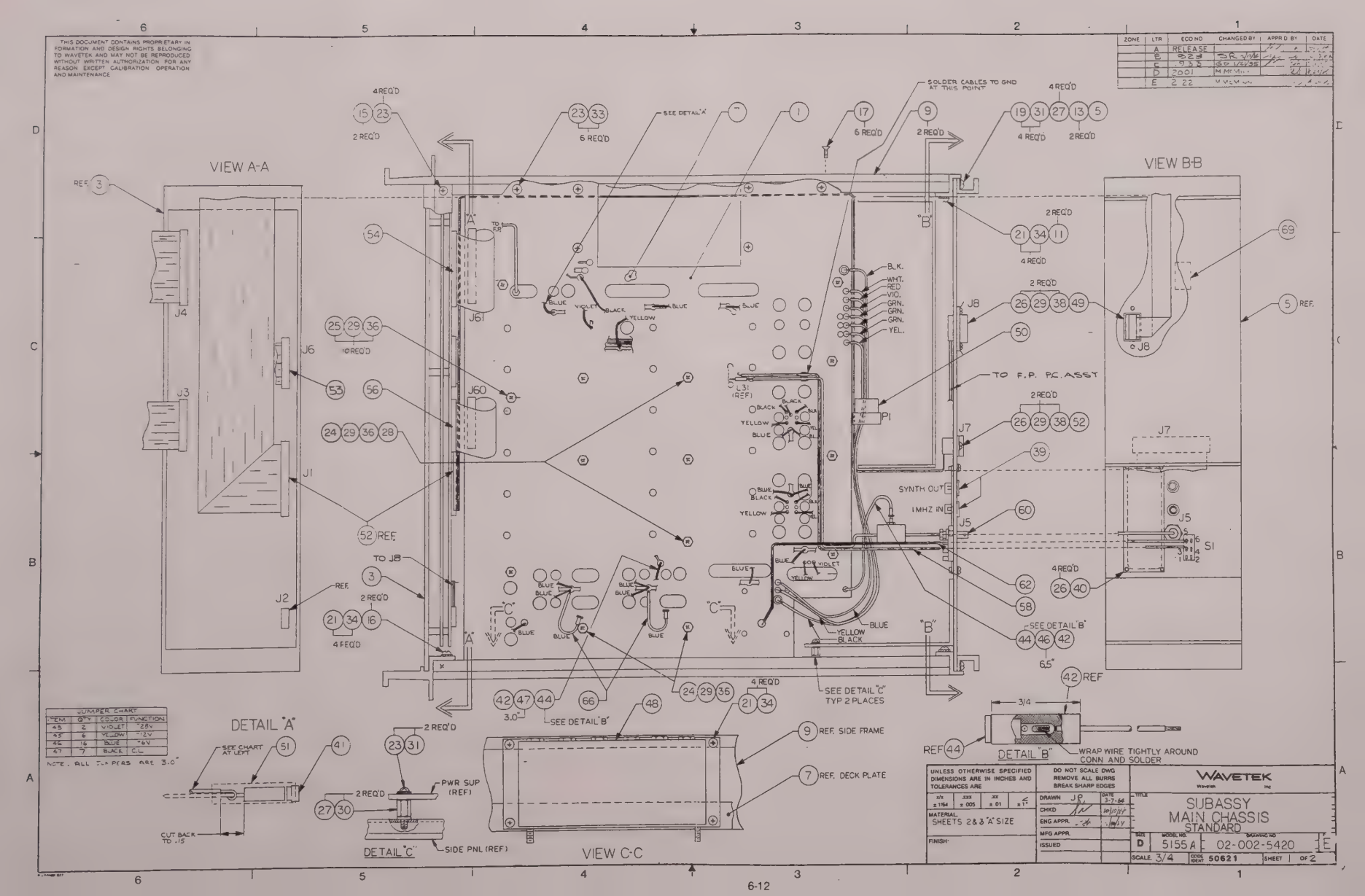
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	323	SR		
	C	355	GO		
	D	2001	M MC		
	E	222	V VE		



JUMPER CHART			
ITEM	QTY	COLOR	FUNCTION
45	2	VIOLET	+28V
45	6	YELLOW	+12V
46	16	BLUE	+6V
47	7	BLACK	C.L.

NOTE: ALL JUMPERS ARE 3.0"

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc
.xx ± .1164 · .xxx ± .005 · .xx ± .01 · ± 1°	DRAWN J.B. DATE 3-7-66	TITLE: SUBASSY MAIN CHASSIS STANDARD
MATERIAL: SHEETS 2 & 3 "A" SIZE	CHKD 10/13/66	
FINISH:	ENG APPR. 10/13/66	
	MFG APPR.	
	ISSUED	SIZE D · MODEL NO. 5155A · DRAWING NO. 02-002-5420 · REV E
		SCALE 3/4 · CODE IDENT 50621 · SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 002 5420 REV E

MAIN CHASSIS SUB ASSY,STD

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	MAINBOARD ASSY, 5150	004.5429	1.00
3	-	PANEL ASSEMBLY FRONT: 5155 STD	001.5420	1.00
5	-	REAR PANEL ASSY: 5150	002.5495	1 00
7	-	DECK PLATE: 5150	304.0715	1.00
9	-	SIDE FRAME: 816	304.0501	2.00
11	-	TRIM: REAR	304.0902	2.00
13	-	CHANNEL: SUPPORT REAR PNL 5600	304.0914	2.00
15	-	TRIM: FRONT TOP SUPR/SNUB 716	307.0914	2.00
16	-	ADAPTOR: RACK MOUNTING	304.0400	2.00
17	-	M SCR: SS PHP 8-32X3/8 100FH	385.8064	6.00
19	-	M SCR: SS PHP 6-32 X 1/2 PH	385.6082	4.00
21	-	M SCR: ST CD PH 8-32 X 3/8 PH	381.8062	12.00
23	-	M SCR: SS PHP 6-32 X 3/8 PH	385.6062	12.00
24	-	M SCR: SS PHP 4-40X7/16 100FH	385.4074	4.00
25	-	M SCR: SS PHP 4-40 X 3/8 100FH	385.4064	10.00
26	-	M SCR: SS PHP 4-40 X 3/8 PH	385.4062	8.00
27	-	WASHER: FLAT STL CAD #6	388.1060	6.00
28	-	SPACER: THD 1/4 HEX X 1.125	376.3004	2.00
29	-	WASHER: SPLT LK STNLS #4	388.1042	20.00
30	-	SPR:THD M/F 5/16HX 6-32 X 7/16	389.2037	2.00
31	-	WASHER: EXT LK STL CAD #6	388.1061	6.00
33	-	WASHER: SPLT LK STNLS #6	388.1062	6.00
34	-	WASHER: EXT LK STL CAD #8	388.1081	12.00
36	-	NUT: HEX SS 4-40 X 1/4AF	387.4081	14.00
38	-	CLIP: CONN RETAIN (351.5006)	362.2102	4.00
39	-	HOLE PLUG: 1/2" PLASTIC BLK	367.1109	2.00
40	-	CONN PLATE BLANKING: (751/752)	303.0910	1.00
41	JUMPERS	SOCKET: LEAD	353.0101	31.00
42	1.5"	SHRINK TBG PLYFIN BLACK 1/4"	378.5540	1.00
43	6"	WIRE: #24 AWG STR VIOLET	378.1774	1.00
44	-	SOCKET: LEAD, .050	353.0111	2.00
45	18"	WIRE: #24 AWG STR YELLOW	378.1744	1.00
46	54-1/2"	WIRE: #24 AWG STR BLUE	378.1764	1.00
47	24"	WIRE: #24 AWG STR BLACK	378.1704	1.00
48	-	FILTER: BANDPASS 874MHZ CAVITY	165.3021	1.00
49	-	CABLE ASSY: 5150 RP-14/FP	009.9544	1.00
50	-	CABLE ASSY: DECK-PS, 5150	009.9547	1.00
51	6"	SHRINK TBG PLYFIN BLACK 1/8"	378.5520	1.00
52	-	CABLE ASSY: 5150 RP-50/FP	009.9541	1.00
53	-	CABLE ASSY: 5150 RP-14/FP	009.9551	1.00
54	-	CABLE ASSY: 5150 MB-50/FP	009.9542	1.00

WAVETEK SD INC. DWG NO. 02 002 5420 REV E

MAIN CHASSIS SUB ASSY,STD

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
56	-	CABLE ASSY: 5150 MB-34/FP	009.9543	1.00
58	-	CABLE ASSY: SGA/RP=P3, 5150	009.0595	1.00
60	-	10MHZ AMP ASSY 5150	002.5467	1.00
62	-	CABLE ASSY: OSC/RP-P5, 5150	009.0597	1.00
64	-	CABLE ASSY: J72/RP-OUT, 5150	009.0827	1.00
66	-	CABLE ASSY: PWR JUMPER 5150	009.5958	2.00
69	-	LABEL: SERIAL NUMBER TAGS	371.1000	1.00

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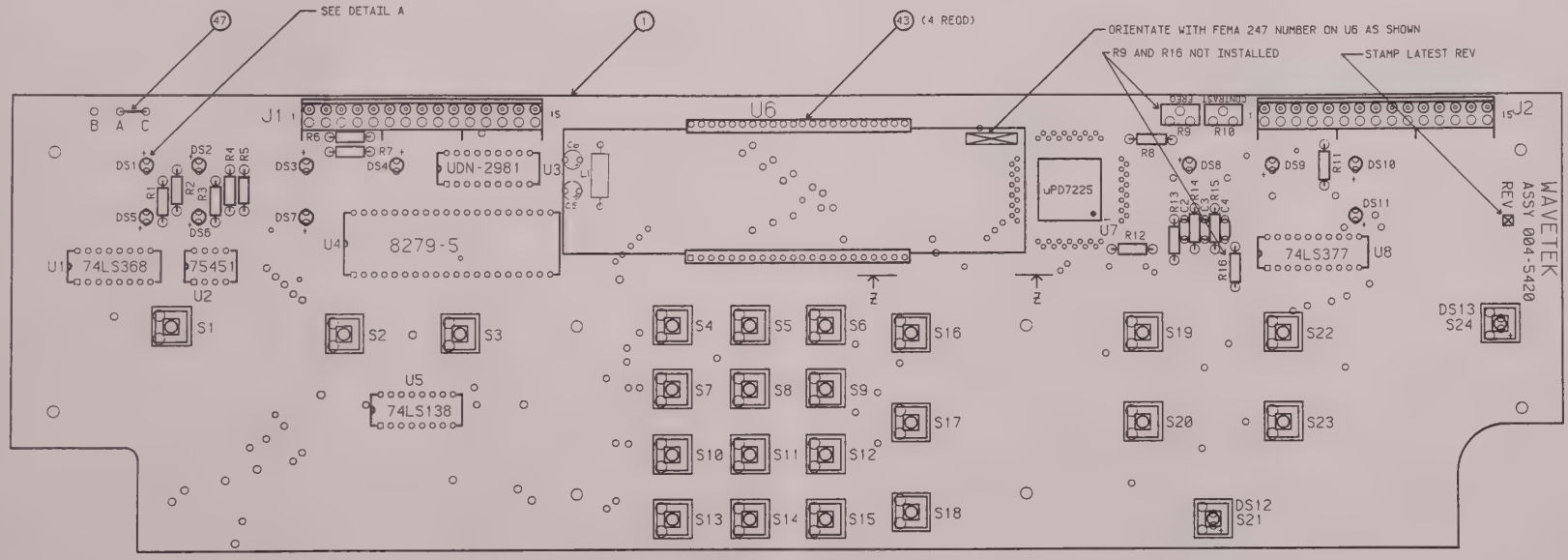
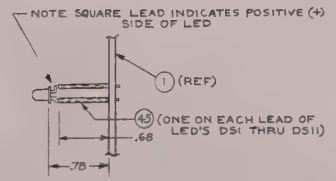
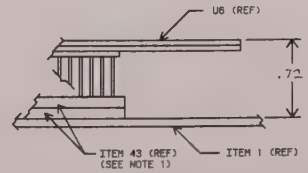
ZONE	LTR	ECO NO	CHANGED BY	APPRD BY	DATE
	A	RELEASE			
	B	ECO 1893	N.P. 9/28/84		
	C	ECO 1981	N.P. 10/9/84		
	D	ECO 1919	N.P. 12/18/84		
	E				





DETAIL A
(TYPICAL MTG OF LED'S)



VIEW Z-Z

NOTE:
1) TO MAINTAIN .72 DIMENSION, CASCADE ITEM 43 TO ITEM 43 SOLDERED TO BOARD. CUT PINS OF U6 BY .10 AND INSTALL U6 INTO SCOKETS.

SHEETS 2 AND 3 ARE "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
X/X ±1/64 | .XXX ±.005 | .XX ±.01 | ∠ ±1°
MATERIAL:
FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

DRAWN	N. PETERS	9/18/84
CHKD		
ENG APPR.		12/5/84
MFG APPR.		
ISSUED		

WAVETEK
Wavetek Rockland Scientific, Inc.

TITLE: P. W. B. ASSEMBLY
KEY BOARD
STANDARD LOCAL

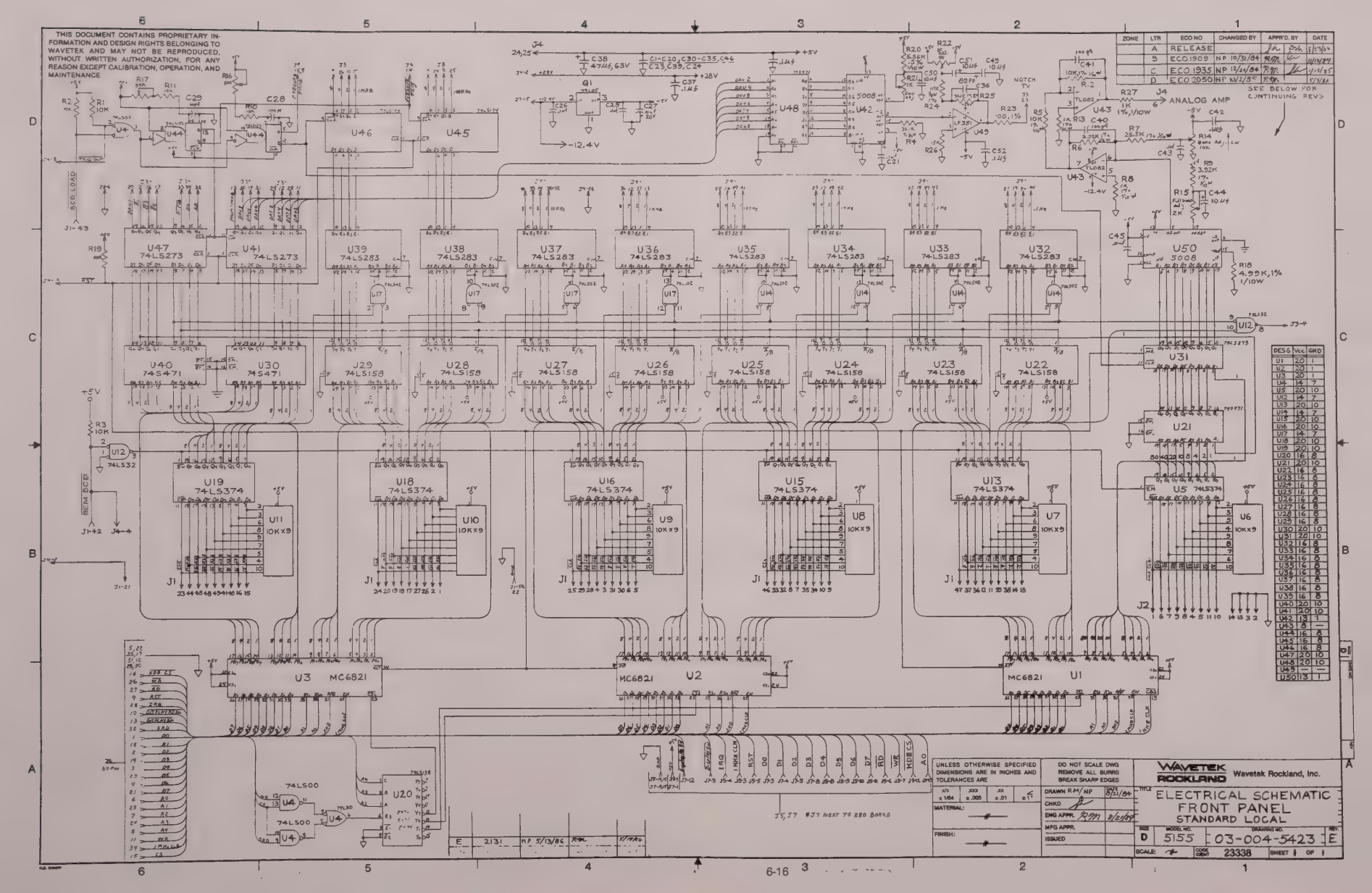
SIZE	MODEL NO.	DRAWING NO.	REV
D	5155	02 - 004 - 5420	E

SCALE: 2:1 | 50621 | SHEET 1 OF 3

WAVETEK SD INC. DWG NO. 02 004 5420 REV E

PC ASSY: DISPLAY/KEYBOARD,STD

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: DISPLAY/KEYBOARD, 5150 ST	320.5420	1.00
3	U1	U: HX BUS DRIV INV 3ST (LS368)	125.0132	1.00
5	U2	U: DUAL PRPHL DRIVER (75451)	120.4451	1.00
7	U3	U: LED DRIVER, NON-INV	120.4081	1.00
9	U4	U: KEY BOARD ENCODER	129.3204	1.00
11	U5	U: 3 TO 8 LINE DECOD (74LS138)	125.0115	1.00
13	U6	DISPLAY: 10 DIGIT LCD .5"	163.4003	1.00
15	U7 [UPD7225]	U: LCD CONTROLLER/DRIVER	120.4025	1.00
17	U8	U:IC 74LS377 OCT LAT	125.0159	1.00
19	S1-S20,22,23,	S: PB SPST N.O. (NON-LTD)	341.1103	22.00
21	S21,S24[DS12,DS13 P/O S21]	SWITCH ASSY: LTD PUSH BTN	008.6101	2.00
23	R1-R7,R11	R: FX CFLM 47 OHM 5% 1/4W	116.0471	8.00
25	R13-R15	R: FX CFLM 47K OHM 5% 1/4W	116.3471	3.00
26	R8	R: FX CFLM 10K OHM 5% 1/4W	116.3101	1.00
27	R10	R: VAR CMT 100K 3/8SQ EM	118.4102	1.00
29	R12	R: FX CFLM 470K OHM 5% 1/4W	116.4471	1.00
31	C2-C4	C: FX MONO 0.1UF Z5U 50V	100.4102	3.00
33	C5,C6,	C: FX TANT 68UF 20% 6V	109.6680	2.00
36	DS1-DS5,DS8-DS11	LED: GRN, MIN. 2MCD@20, 68OVA	171.1604	9.00
37	DS6,DS7	LED: RED, MIN. 2MCD@10, 70OVA	171.1603	2.00
39	L1,	L: FXD 1 MHY +/-10% SHLD	150.2100	1.00
41	J1,J2	SOCKET: 15 PIN SIL ST .156	353.1501	2.00
43	-	SOCKET: 22PIN SIL ST	353.2202	4.00
45	DS1-DS11	SLVNG: TEFLON #28AWG	378.5202	15.00
47	6"	WIRE: #30 AWG SLD KYN BLUE	378.1961	1.00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ZONE | LTR | ECO NO | CHANGED BY | APPR'D. BY | DATE
A | RELEASE
B | ECO 1909 | NP 10/31/84
C | ECO 1935 | NP 12/21/84
D | ECO 2050 | NP 11/2/85
SEE BELOW FOR CONTINUING REVS
ANALOG AMP
U1 MC6821
U2 MC6821
U3 MC6821
U50 5008
DESG | Vcc | GND
ELECTRICAL SCHEMATIC
FRONT PANEL
STANDARD LOCAL
WAVETEK ROCKLAND
Wavetek Rockland, Inc.
MODEL NO. 5155
DRAWING NO. 03-004-5423
REV. E
SIZE D
SCALE:
CODE IDENT 23338
SHEET 1 OF 1
DRAWN R.M/NP 8/21/84
CHKD
ENG APPR. 8/21/84
MFG APPR.
ISSUED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES
MATERIAL:
FINISH:
J5,J7 #37 NEXT TO Z80 BOARD
6-16

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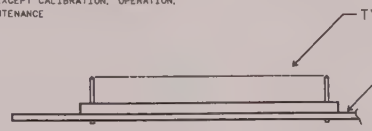
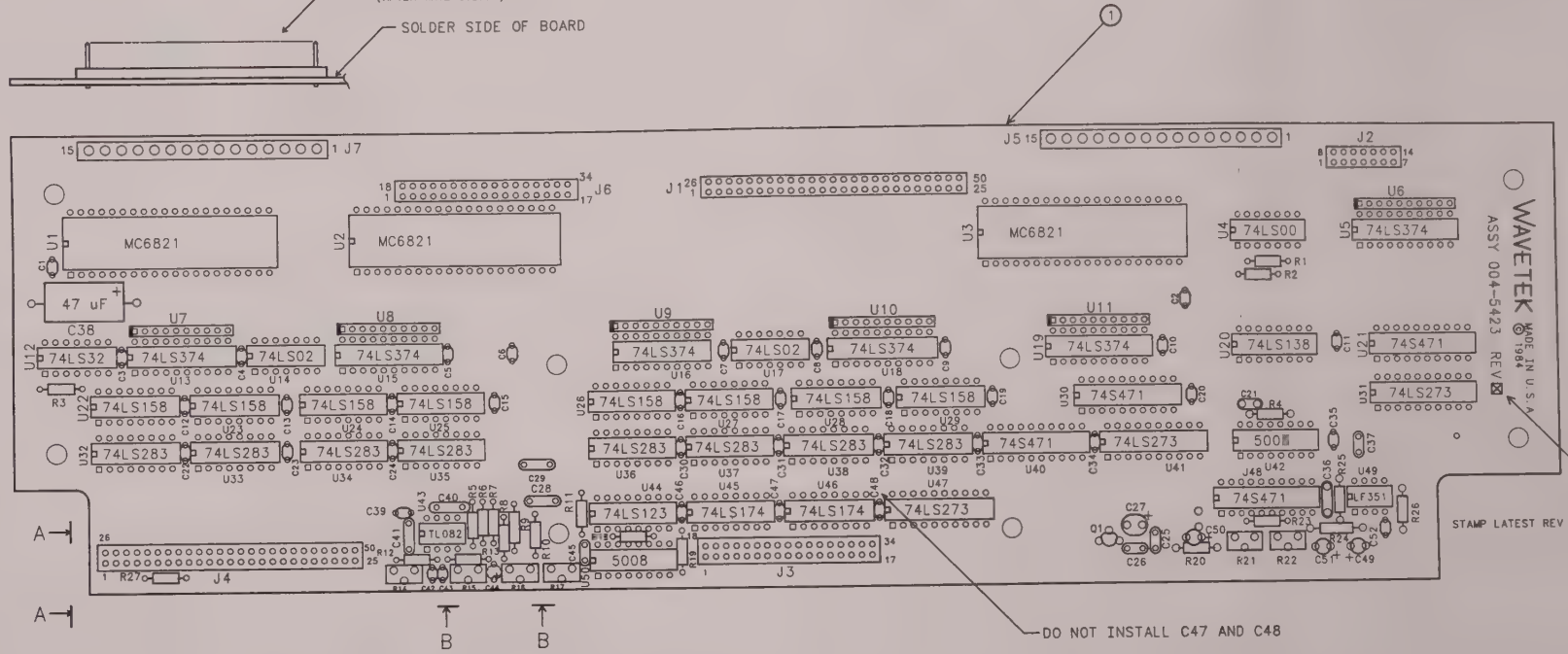
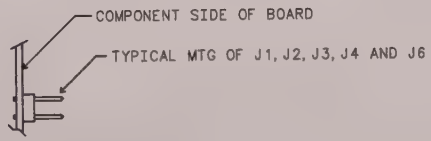
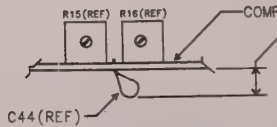
ZONE	LTR	ECO NO	CHANGED BY	APPRD BY		DATE
	A	RELEASE				
	B	ECO 1909	M.P. 10/28/84			
	C	ECO 1921	M.P. 11/25/84			
	D	ECO 1935	M.P. 12/20/84	R.M.	S.R	1/15/85
	E	ECO 2050	M.P. 10/17/85	R.M.		5/12/86
	F	ECO 2131	M.P. 5/13/86	J.T.		







VIEW A–A



VIEW B–B

SHEETS 2 TO 4 ARE "A" SIZE L/M

NOTE:
1) ALL COMPONENTS TO BE FLUSH WITH PRINTED WIRING BOARD.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc
X/± 1/64 | XXX ± .005 | XX ± .01 | ∠ ± 1°	DRAWN N PETERS 7/31/84	TITLE: P.C. ASSEMBLY FRONT PANEL STANDARD LOCAL
MATERIAL:	CHKD	
	ENG APPR. R M. 1/15/85	
FINISH:	MFG APPR.	SIZE D | MODEL NO. 5155 | DRAWING NO. 02 – 004 – 5423 | F
	ISSUED	SCALE: 2:1 | 23338 | SHEET 1 OF 4

WAVETEK SD INC. DWG NO. 02 004 5423 REV D

PC ASSY: FRONT PANEL (5155A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	@	PWB: FRONT PANEL, 5150 (STD)	320.5423	1.00
3	U1,U2,U3	U: MC6821	127.6821	3.00
5	U4	U: QUAD 2 IN NAND GATE	125.7400	1.00
7	U5,U31,U41,U47	U: OCT D-FLIP W/CLR (74LS273)	125.0139	4.00
9	U12	U: QUAD 2 IN OR GATE	125.7432	1.00
11	U13,U15,U16,U18,U19	U: OCT D-FLIP 3-ST (74LS374)	125.0140	5.00
13	U14,U17	U: QUAD 2IN NOR GATE	125.7402	2.00
14	U21	PROM: PGMD U6-5416 (129.3012)	021.1025	1.00
15	U20	U: 3 TO 8 LINE DECOD (74LS138)	125.0115	1.00
16	U30	PROM: PGMD U15-5422 (129.3012)	021.1022	1.00
17	U40	PROM: PGMD U16-5422 (129.3012)	021.1023	1.00
18	U48	PROM: PGMD U64-5422 (129.3012)	021.1024	1.00
19	U22 THRU U29	U: QD 2 TO 1 INV MUX (74LS158)	125.0149	8.00
21	U32-U39	U: 4 BT FULL ADDER (74LS283)	125.0130	8.00
23	U42,U50	DAC: 8 BIT BINARY	129.1505	2.00
25	U43	U: DL LIN BIFET OP-AMP (TL082C	120.2002	1.00
27	U49	U: LIN BIFET OP-AMP DIL LF351	120.1017	1.00
29	U6,U7,U8,U9,U10,U11	U: PULL UP NET 10K 2% X9 SIP	128.3104	6.00
31	U44	U: DL MNSTBL MULTVIB (74LS123)	125.0107	1.00
33	U45,U46	U: HX TYPE D FLIP FLOP 74LS174	125.0109	2.00
35	R1-R3,R10,R11,R19	R: FX CFLM 10K OHM 5% 1/4W	116.3101	6.00
37	R4,R25	R: FX MFLM 30.1K 1% 1/10W T2	112.3011	2.00
41	R6	R: FX MFLM 2.72K 1% 1/8W T0	111.2720	1.00
43	R5,R7,R12	R: FX MFLM 10.0K 1% 1/10W T2	112.1001	3.00
45	R8,R13,R27,R23	R: FX MFLM 1.00K 1% 1/10W T2	111.1001	4.00
47	R9	R: FX MFLM 3.92K 1% 1/10W T2	111.3921	1.00
49	R18	R: FX MFLM 4.99K 1% 1/10W T2	111.4991	1.00
51	R20	R: FX MFLM 5.56K .5% 1/10W T2	111.5561	1.00
53	R24	R: FX MFLM 117K 1% 1/8W T0	113.1170	1.00
55	R26	R: FX CFLM 15K OHM 5% 1/4W	116.3151	1.00
57	R14	R: VAR CMT 10K 3/8SQ EM	118.3103	1.00
58	R15	R: VAR CMT 2.0K 3/8SQ EM	118.2203	1.00
59	R21	R: VAR CMT 1.0K 3/8SQ EM	118.2101	1.00
61	R16,R17	R: VAR CMT 50K 3/8SQ EM	118.3500	2.00
63	R22	R: VAR CMT 5.0K 3/8SQ EM	118.2501	1.00
65	C45	C: FX MONO .01UF +80 -20% 50V	100.3105	1.00
67	C46,C43,C44,C49-C52	C: FX MONO 0.1UF Z5U 50V	100.4102	0.00
67	C1-C26,C30-C35,C37,C39,C42,	C: FX MONO 0.1UF Z5U 50V	100.4102	42.00
69	C27	C: FX TANT 10UF 20% 20V	109.6100	1.00
71	C28-C29,C40-C41	C: FX MICA DP 100PF +-5% 500V	101.1100	4.00
73	C36	C: FX MICA DP 470PF +-5% 500V	101.1470	1.00

WAVETEK SD INC. DWG NO. 02 004 5423 REV D

PC ASSY: FRONT PANEL (5155A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
75	C38	C: FX ELECT 47UF 20% 63V	109.6470	1.00
77	Q1	Q: N.V. REG 5V (79L05)	120.0054	1.00
79	J6,J3	CONN: TERM 34 PIN DIL ST	354.0005	2.00
81	J1,J4	CONN: TERM 50PIN DIL ST	354.0021	2.00
83	J5,J7	CONN: TERM 15 PIN SIL ST .156	354.0039	2.00
85	J2	CONN: TERM 14 PIN DIL ST	354.0031	1.00

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ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	REL 4.3.5			7/6/84
	B	ECO 1913	MP 11/15/84	RGM	11/16/84

EPROM JUMPER

8K 2764	1&5
16K 27128	1,3&5
32K 27256	2,3&5

TB1

DESG	Vcc	GND
U1	11	29
U2	14	7
U3	14	7
U4	14	7
U5	14	7
U6	14	7
U7	14	7
U8	16	8
U9	5	10
U10	14	7
U11	14	7
U12	14	7
U13	20	10
U14	20	10
U15	20	10
U16	20	10
U17	24	12
U18	28	14

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES		
X/± 1/64	XXX ± .005	XX ± .01	∠ ±1°	DRAWN M. McMINN	DATE 7/2/84	WAVETEK Wavetek Rockland Scientific Inc
MATERIAL: —				CHKD		TITLE ELECTRICAL SCHEMATIC Z80 BOARD
FINISH —				ENG APPR. RGM	11/16/84	
				MFG APPR.	7/6/84	SIZE D MODEL NO. 5150 DRAWING NO. 03-004-5413 REV B
				ISSUED		SCALE: — CODE IDENT 50621 SHEET OF

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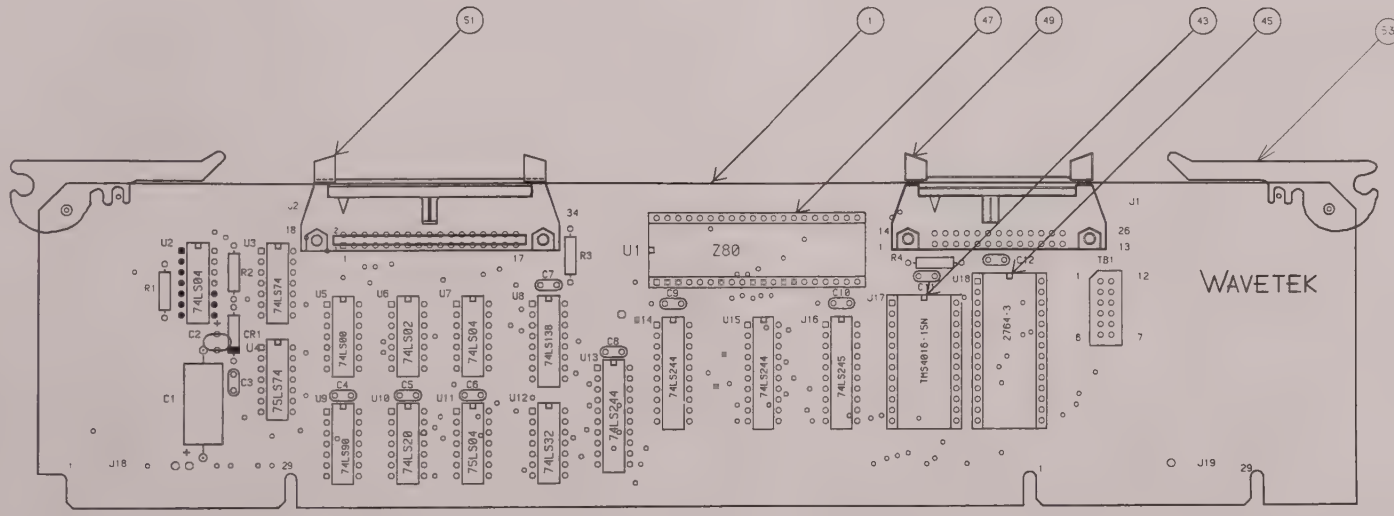
ZONE	LTR	ECO NO.	CHANGED BY	APPRD BY	DATE

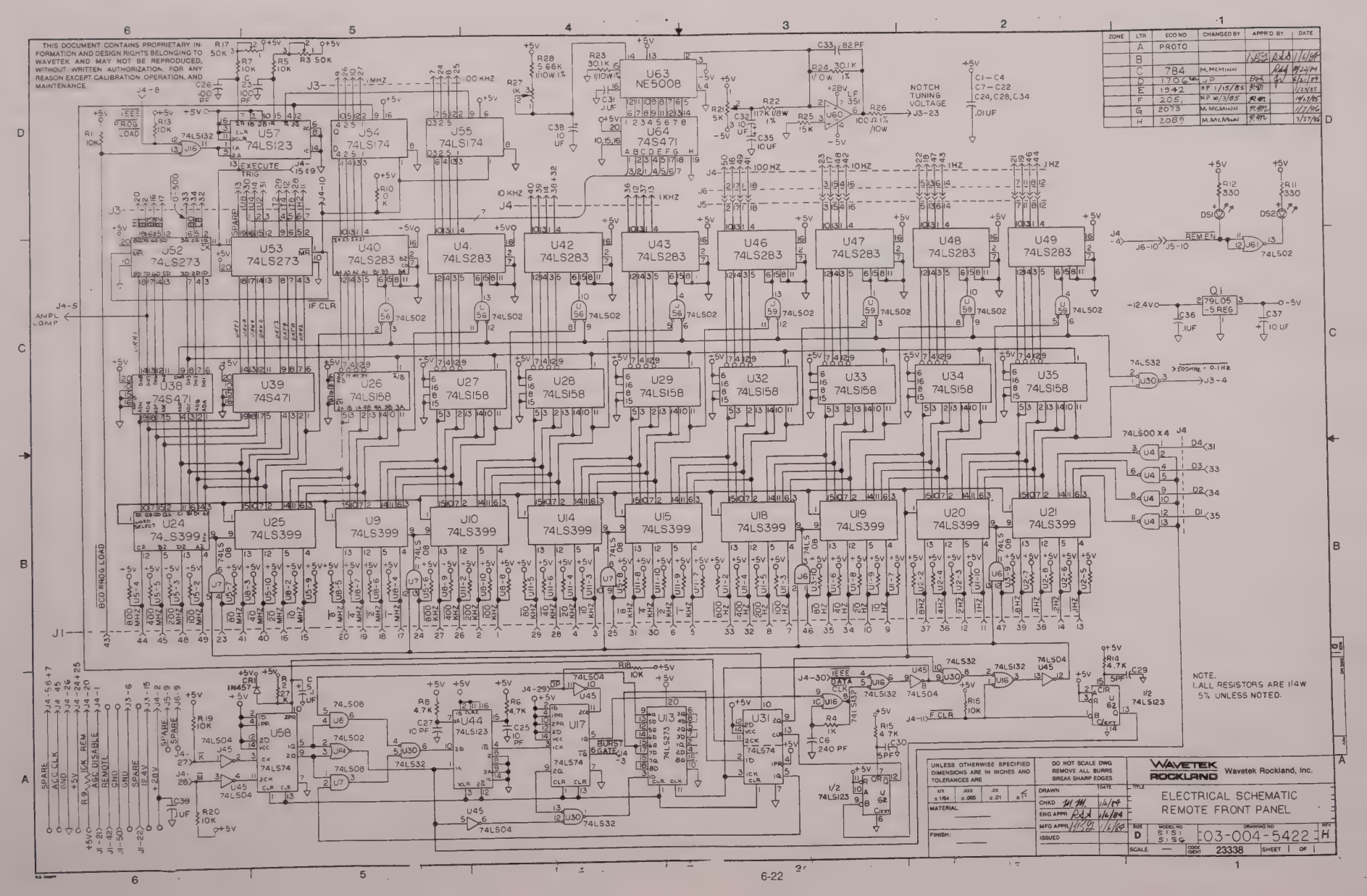


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: X/X ±1/64 ; .XXX ±.005 ; .XX ±.01 ; ∠ ±1	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific, Inc.	
MATERIAL: SHEETS 2&3 "A" SIZE	DRAWN P.	TITLE: P.C. ASSEMBLY Z80	
FINISH:	CHKD		
	ENG APPR	SIZE: D	MODEL NO: 5150
	MFG APPR	SCALE: 2:1	DRAWING NO: 02-004-5413
	ISSUED	50621	SHEET 1 OF 3

WAVETEK SD INC. DWG NO. 02 004 5413 REV B

PC ASSY: Z80 PROCESSOR

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: Z80 PROCESSOR, 5150 STD	320.5413	1.00
3	U1	U: MICROPROCESSOR(2MHZ, Z80)	129.3201	1.00
5	U2,U7,U11	U: HEX INVERTER	125.7404	3.00
7	U13,U14,U15	U: OCT BUF 3-ST (74LS244)	125.0153	3.00
9	U3,U4	U: DUAL TYPE D FLIP FLOP	125.7474	2.00
11	U5	U: QUAD 2 IN NAND GATE	125.7400	1.00
13	U6	U: QUAD 2IN NOR GATE	125.7402	1.00
15	U8	U: 3 TO 8 LINE DECOD (74LS138)	125.0115	1.00
17	U9	U: DECADE COUNTER	125.7490	1.00
19	U10	U: DUAL 4 IN NAND GATE	125.7420	1.00
21	U12	U: QUAD 2 IN OR GATE	125.7432	1.00
23	U16	U: OCT BUS XCVR 3ST (74LS245)	125.0154	1.00
25	U17	U: SRAM 2048 X 8 NMOS	129.3032	1.00
27	U18	EPOM: PGMD U18-5413 (129.3034)	021.3560	1.00
29	R1	R: FX CFLM 470 OHM 5% 1/4W	116.1471	1.00
31	R2,R4	R: FX CFLM 10K OHM 5% 1/4W	116.3101	2.00
33	R3	R: FX CFLM 1.0K OHM 5% 1/4W	116.2101	1.00
35	C1	C: FX ELECT 47UF 20% 63V	109.6470	1.00
37	C2	C: FX TANT 10UF 20% 20V	109.6100	1.00
39	C3 THRU C12	C: FX MONO 0.1UF Z5U 50V	100.4102	10.00
41	CR1	CR: SL LW LK 70PIV 200MW 1N457	132.0457	1.00
43	XU17	SOCKET: IC 24PIN DIP ST	353.2402	1.00
45	XU18	SOCKET: IC 28PIN DIP ST	353.2800	1.00
47	FOR U1	SOCKET: IC 40PIN DIP ST	353.4001	1.00
49	J1	PLUG: HDR 26P DIL RT ANG ST LK	352.2601	1.00
51	J2	PLUG: HDR 34P DIL RT ANG ST LK	352.3400	1.00
53	-	EJECTOR: PC, 5830	364.0404	2.00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ZONE | LTR | ECO NO | CHANGED BY | APPR'D BY | DATE
A PROTO
C 784 M.MCMINN
D 1700 J.P
E 1942 RP 1/15/85
F 205 NP 10/3/85
G 2073 M.MCMINN
H 2089 M.MCMINN
U63 NE5008
U64 74S471
U57 74LS123
U54 74LS174
U55 74LS174
U53 74LS273
U52 74LS273
U40 74LS283
U4. 74LS283
U42 74LS283
U43 74LS283
U46 74LS283
U47 74LS283
U48 74LS283
U49 74LS283
U39 74S471
U38 74S471
U26 74LS158
U27 74LS158
U28 74LS158
U29 74LS158
U32 74LS158
U33 74LS158
U34 74LS158
U35 74LS158
U24 74LS399
U25 74LS399
U9 74LS399
U10 74LS399
U14 74LS399
U15 74LS399
U18 74LS399
U19 74LS399
U20 74LS399
U21 74LS399
U58 74LS74
U44 74LS123
U7 74LS74
U3 74LS273
U31 74LS74
U45 74LS04
U30 74LS32
U16 74LS32
U62 74LS123
Q1 79L05 -5 REG
NOTE. 1. ALL RESISTORS ARE 1/4W 5% UNLESS NOTED.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES
DRAWN
CHKD
ENG APPR
MFG APPR
ISSUED
MATERIAL
FINISH:
WAVETEK ROCKLAND Wavetek Rockland, Inc.
ELECTRICAL SCHEMATIC REMOTE FRONT PANEL
SIZE D MODEL NO 5151 5152 DRAWING NO 03-004-5422 REV H
SCALE — CODE IDENT 23338 SHEET 1 OF 1

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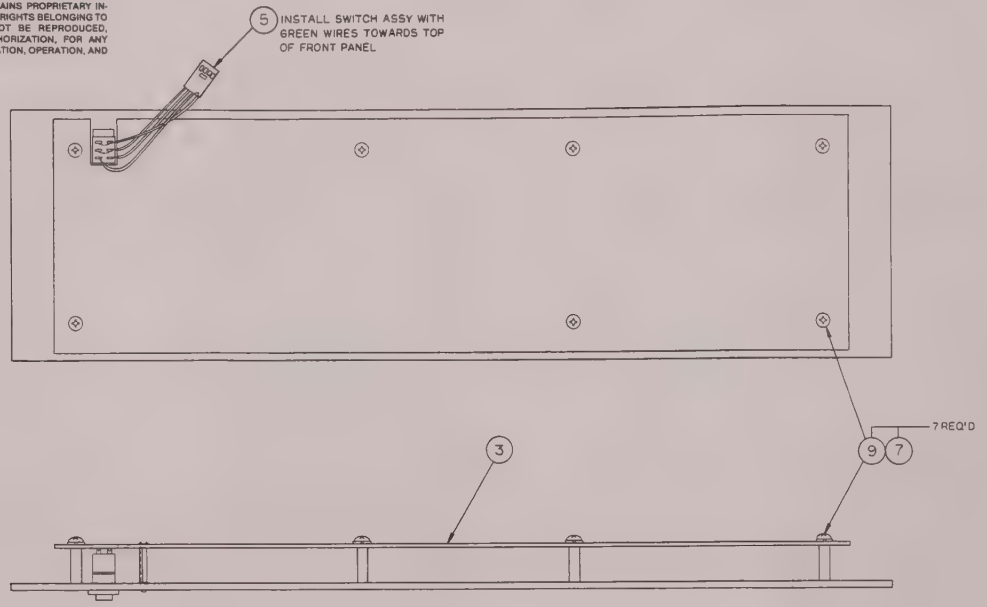
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			1-6-84



SHEET 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.	
X/X ± 1/64 .XXX ± .005 .XX ± .01 ∠ ± 1°	DRAWN: M McMinn DATE 9/26/83	TITLE FRONT PANEL ASSY REMOTE	
MATERIAL	CHKD DATE 11/6/89		
	ENG APPR. DATE 1-6-84		
FINISH	MFG APPR. DATE 1-6-84	MODEL NO. 5150	DRAWING NO. 02-001-5422 REV A
	ISSUED	SCALE 1:1	CODE IDENT 50621 SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 001 5422 REV A

PANEL ASSY: FRONT,REMOTE (5155A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	FRONT PANEL: 5150 (REM)	300.5422	1.00
3	-	FRONT PANEL ASSY, 5150 (REM)	004.5422	1.00
5	-	CABLE ASSY: RP-FP POWER, 5150	009.9540	1.00
7	-	M SCR: ST CD PH 6-32 X 3/8 PH	381.6062	7.00
9	-	WASHER: SPLT LK STNLS #6	388.1062	7.00

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ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	704			
	C	1884			
	D	1929	BR	DM	9/3/84
	E	1933	GD	DM	11-1-84
	F	2001	M McMINN		4/15/85
	G	2.22	M McMINN		4/25/85

VIEW A-A

VIEW B-B

VIEW C-C

DETAIL "A"

DETAIL "B"

DETAIL "C"

JUMPER CHART			
ITEM	QTY	COLOR	FUNCTION
45	2	VIOLET	+28V
45	6	YELLOW	+12V
46	16	BLUE	+6V
47	7	BLACK	C.L.

(NOTE: ALL JUMPERS ARE 3.0")

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: X/64 ±1/64, .XXX ±.005, .XX ±.01, ±1°

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

MATERIAL: SHEETS 2 & 3 "A" SIZE

FINISH: 11

		DATE
DRAWN	JP	3-7-84
CHK'D		11/2/84
ENG APPR.		11/17/84
MFG APPR.		
ISSUED		

WAVETEK
Wavetek Rockland Scientific Inc

TITLE: SUBASSY MAIN CHASSIS REMOTE

SIZE	MODEL NO	DRAWING NO	REV
D	515GA	02-002-5422	JG

SCALE: 3/4 | CODE IDENT: 50621 | SHEET 1 OF 2

6-25

WAVETEK SD INC. DWG NO. 02 002 5422 REV F

MAIN CHASSIS ASSY: REMOTE

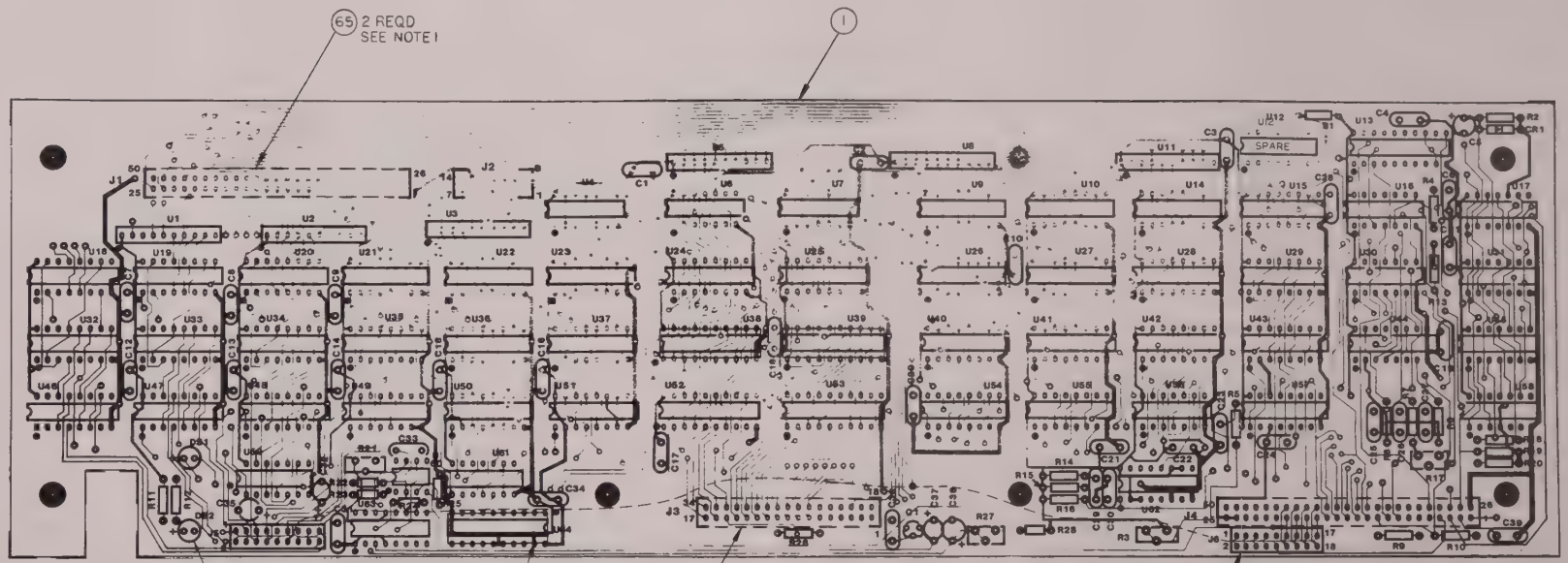
ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	MAINBOARD ASSY, 5150	004.5429	1.00
3	-	PANEL ASSEMBLY FRONT: 5156 REM	001.5422	1.00
5	-	REAR PANEL ASSY: 5150	002.5495	1.00
7	-	DECK PLATE: 5150	304.0715	1.00
9	-	SIDE FRAME: 816	304.0501	2.00
11	-	TRIM: REAR	304.0902	2.00
12	-	M SCR: SS PHP 6-32 X 3/8 PH	385.6062	12.00
13	-	CHANNEL: SUPPORT REAR PNL 5600	304.0914	2.00
15	-	TRIM: FRONT TOP SUPR/SNUB 716	307.0914	2.00
17	-	M SCR: SS PHP 8-32X3/8 100FH	385.8064	6.00
19	-	M SCR: SS PHP 6-32 X 1/2 PH	385.6082	4.00
21	-	M SCR: ST CD PH 8-32 X 3/8 PH	381.8062	12.00
25	-	M SCR: SS PHP 4-40 X 3/8 100FH	385.4064	10.00
26	-	M SCR: SS PHP 4-40 X 3/8 PH	385.4062	8.00
27	-	WASHER: FLAT STL CAD #6	388.0060	6.00
28	-	SPACER: THD 1/4 HEX X 1.125	376.3004	2.00
29	-	WASHER: SPLT LK STNLS #4	388.1042	20.00
30	-	SPR:THD M/F 5/16HX 6-32 X 7/16	389.2037	2.00
31	-	WASHER: EXT LK STL CAD #6	388.1061	6.00
33	-	WASHER: SPLT LK STNLS #6	388.1062	6.00
34	-	WASHER: EXT LK STL CAD #8	388.1081	12.00
36	-	NUT: HEX SS 4-40 X 1/4AF	387.4081	14.00
38	-	CLIP: CONN RETAIN (351.5006)	362.2102	4.00
39	-	HOLE PLUG: 1/2" PLASTIC BLK	367.1109	1.00
40	-	CONN PLATE BLANKING: (751/752)	303.0910	1.00
41	JUMPERS	SOCKET: LEAD	353.0101	31.00
42	6"	SHRINK TBG PLYFIN BLACK 1/4"	378.5540	1.00
43	6"	WIRE: #24 AWG STR VIOLET	378.1774	1.00
44	-	SOCKET: LEAD, .050	353.0111	2.00
45	18"	WIRE: #24 AWG STR YELLOW	378.1744	1.00
46	54-1/2"	WIRE: #24 AWG STR BLUE	378.1764	1.00
47	24"	WIRE: #24 AWG STR BLACK	378.1704	1.00
48	-	FILTER: BANDPASS 874MHZ CAVITY	165.3821	1.00
49	-	CABLE ASSY: 5150 700-34/FP	009.9552	1.00
50	REF. P1	CABLE ASSY: DECK-PS, 5150	009.9547	1.00
52	-	CABLE ASSY: 5150 RP-50/FP	009.9541	1.00
54	-	CABLE ASSY: 5150 MB-50/FP	009.9542	1.00
56	-	CABLE ASSY: 5150 MB-34/FP	009.9543	1.00
58	-	CABLE ASSY: SGA/RP-P3, 5150	009.0595	1.00
60	-	10MHZ AMP ASSY 5150	002.5467	1.00

WAVETEK SD INC. DWG NO. 02 002 5422 REV F

MAIN CHASSIS ASSY: REMOTE

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
62	-	CABLE ASSY: OSC/RP-PS, 5150	009.0597	1.00
64	-	CABLE ASSY: J72/RP-OUT, 5150	009.0827	1.00
66	-	CABLE ASSY: PWR JUMPER 5150	009.9550	2.00
68	-	CONN: BNC BLKHD, RIGID COAX	351.0025	1.00
69	-	LABEL: SERIAL NUMBER TAGS	371.1000	1.00

ZONE	LTR	ECO NO	CHANGED BY	APPRD BY	DATE
	A				
	B	1784			3/14/89
	C				
	D	2089			3/27/96


65 2 REQD SEE NOTE 1
1
SPARE
61 LONGER LEAD DENOTES ANODE (+) TYP CR2 + CR3
68 3 REQ'D
67 SEE NOTE 1
64 66 SEE NOTE 3
2 REQD
13/16
63 CUT AND INSTALL AS SHOWN (2 PLS)

NOTE

1- CONNECTORS J1, J3 + J4 ARE INSTALLED ON SOLDER SIDE OF BOARD

2- U22, U23, U36, U37, U50, U51 + J2 ARE NOT USED ON THIS ASSY

3- ON COMPONENT SIDE OF BOARD, WIRE WRAP J5-1 TO J6-1, J5-2 TO J6-2 ETC (NOTE J5-9 TO J6-9 IS NOT CONN. AT THIS TIME)

SHT 2+3 ARE "A" SIZE L/M

DR M.M. Mann	DATE 1/4-89	WAVETEK ROCKLAND Wavetek Rockland, Inc.
CHKD M.M.	1/6/89	
ENG R.A.S.	1-6-89	PC ASSY
MFG [illegible]	1-6-89	REMOTE FRONT PANEL
ISSUED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

MAT —

FIN —

SIZE	MODEL NO	DRAWING NO	REV
D	5151 5156	102 004 5422	D
SCALE 2:1	CODE IDENT 23338	SHEET 1 OF 3	

WAVETEK SD INC. DWG NO. 02-004-5422 REV D

PC ASSY: FRONT PANEL (5156A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: FRONT PANEL, 5150 (REM)	320.5422	1.00
3	U1,U2,U3,U5,U8,U11	U: PULL UP NET 10K 2% X9 SIP	128.3104	6.00
5	[illegible]	U: QUAD 2 IN NAND GATE	125.7400	1.00
7	U6,U7	U: QUAD 2 IN AND GATE	125.7408	2.00
9	U9,U10,U14,U15,U18 THRU U21	U: QUAD 2 PORT REG (74LS399)	125.0152	10.00
9	,U24,U25	U: QUAD 2 PORT REG (74LS399)	125.0152	0.00
11	U63	DAC: 8 BIT BINARY	129.1505	1.00
13	U13,U52,U53	U: OCT D-FLIP W/CLR (74LS273)	125.0139	3.00
14	U68	U: LIN BIFET OP-AMP DIL LF351	128.1017	1.00
15	U16	U: QD 2IN NAND SMT TGR (LS132)	125.0148	1.00
17	U17,U31,U58	U: DUAL TYPE D FLIP FLOP	125.7474	3.00
19	U26 THRU U29,U32 THRU U35	U: QD 2 TO 1 INV MUX (74LS158)	125.0149	8.00
21	[illegible]	U: QUAD 2 IN OR GATE	125.7432	1.00
22	U64	PROM: PGMD U64-5422 (129.3012)	021.1024	1.00
23	[illegible]	PROM: PGMD U16-5422 (129.3012)	021.1023	1.00
24	U39	PROM: PGMD U15-5422 (129.3012)	021.1022	1.00
25	U40 THRU U43,U46 THRU U49	U: 4 BT FULL ADDER (74LS283)	125.0130	8.00
27	U44,U57,U62	U: DL MNSTBL MULTVIB (74LS123)	125.0107	3.00
29	U45	U: HEX INVERTER	125.7404	1.00
31	U54,U55	U: HX TYPE D FLIP FLOP 74LS174	125.0109	2.00
33	U56,U59,U61	U: QUAD 2IN NOR GATE	125.7402	3.00
34	R27	R: VAR CMT 1.0K 3/8SQ EM	118.2101	1.00
35	R1,R5,R7,R9,R10,R13,R16,R18	R: FX CFLM 10K OHM 5% 1/4W	116.3101	10.00
35	,R19,R20	R: FX CFLM 10K OHM 5% 1/4W	116.3101	0.00
36	R28	R: FX MFLM 5.56K .5% 1/10W T2	111.5561	1.00
37	R2	R: FX CFLM 27K OHM 5% 1/4W	116.3271	1.00
38	R25	R: FX CFLM 15K OHM 5% 1/4W	116.3151	1.00
39	R3,R17	R: VAR CMT 50K 3/8SQ EM	118.3500	2.00
40	R23,R24	R: FX MFLM 30.1K 1% 1/10W T2	112.3011	2.00
41	R4	R: FX CFLM 1.8K OHM 5% 1/4W	116.2101	1.00
42	R22	R: FX MFLM 117K 1% 1/8W T0	113.1170	1.00
43	R6,R8,R14,R16	R: FX CFLM 4.7K OHM 5% 1/4W	116.2471	4.00
44	R21	R: VAR CMT 5.0K 3/8SQ EM	118.2501	1.00
45	R11,R12	R: FX CFLM 330 OHM 5% 1/4W	116.1331	2.00
46	R26	R: FX MFLM 100 OHM 1% 1/10W T2	110.1001	1.00
47	C1 THRU C4,C7 THRU C22,C24	C: FX MONO .01UF +80 -20% 50V	100.3105	22.00
47	,C28	C: FX MONO .01UF +80 -20% 50V	100.3105	0.00
48	C31,C34,C36,C39	C: FX MONO 0.1UF ZSU 50V	100.4102	4.00
49	C5	C: FX TANT .10UF 20% 35V	109.4100	1.00
50	C32,C35,C37,C38	C: FX TANT 10UF 20% 20V	109.6100	4.00
51	C6	C: FX MICA DP 240PF +-5% 500V	101.1240	1.00

WAVETEK SD INC. DWG NO. 02-004-5422 REV D

PC ASSY: FRONT PANEL (5156A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
51	AS REQ.	SHRINK TBG PLYFIN BLACK 1/8"	378.5520	1.00
53	C23,C26	C: FX CER 100PF 10% X5F 500V	100.1105	2.00
55	C25,C27	C: FX CER 10PF 5% NPO 500V	100.0109	2.00
56	C33	C: FX MICA DP 82PF +-5% 500V	101.0820	1.00
57	C29,C30	C: FX MICA DP 5PF +-.5PF 500V	101.0050	2.00
58	Q1	Q: N.V. REG 5V (79L05)	120.0054	1.00
59	CR1	CR: SL LW LK 70PIV 200MW 1N457	132.0457	1.00
61	DS1,DS2	LED: RED DIF. 0.8MCD@20	171.1605	2.00
63	FOR CR2 & CR3	SLVNG: TEFLON #20AWG	378.5202	1.50
64	QTY IN INCHES	WIRE: #30 AWG SLD KYN BLUE	378.1961	162.00
65	J1,J4	CONN: TERM 50PIN DIL ST	354.0021	2.00
66	J5,J6	CONN: TERM 18 PIN DIL ST	354.0038	2.00
67	J3	CONN: TERM 34 PIN DIL ST	354.0005	1.00
68	FOR U38,U39,U64	SOCKET: IC 20PIN DIP ST	353.2001	3.00

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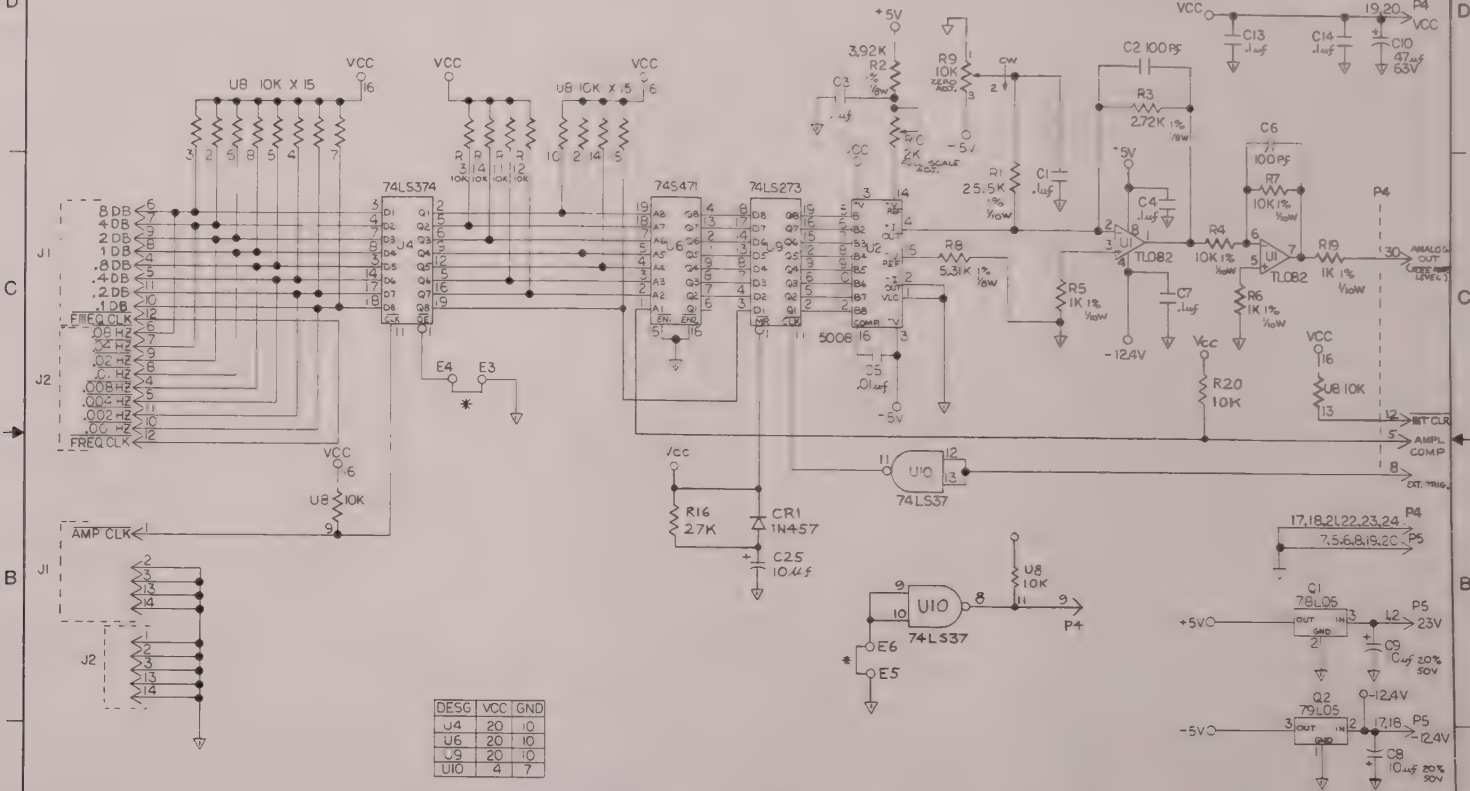
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			10-4-84
	B	ECO 1920			11-23-84
	C	ECO 2043	M. PORTER		10/28/85
	D	2105	M. McMINN		1/19/86



DESG	VCC	GND
U4	20	10
U6	20	10
U9	20	10
U10	4	7

NOTE: ALL RESISTORS ARE 5% 1/4W UNLESS OTHERWISE NOTED

* ADD JUMPER FOR BCD ASSY.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

WAVETEK
Wavetek Rockland Scientific, Inc

DRAWN	J P	10/1/84
CHKD		10/4/84
ENG APPR		10-2-84
MFG APPR		
ISSUED		

MATERIAL

FINISH

TITLE: SCHEMATIC BCD AMP.

SIZE	MODEL NO	DRAWING NO	REV
C	5150	03-004-5417	D

SCALE NONE | CODE IDENT 50621 | SHEET 1 OF 1

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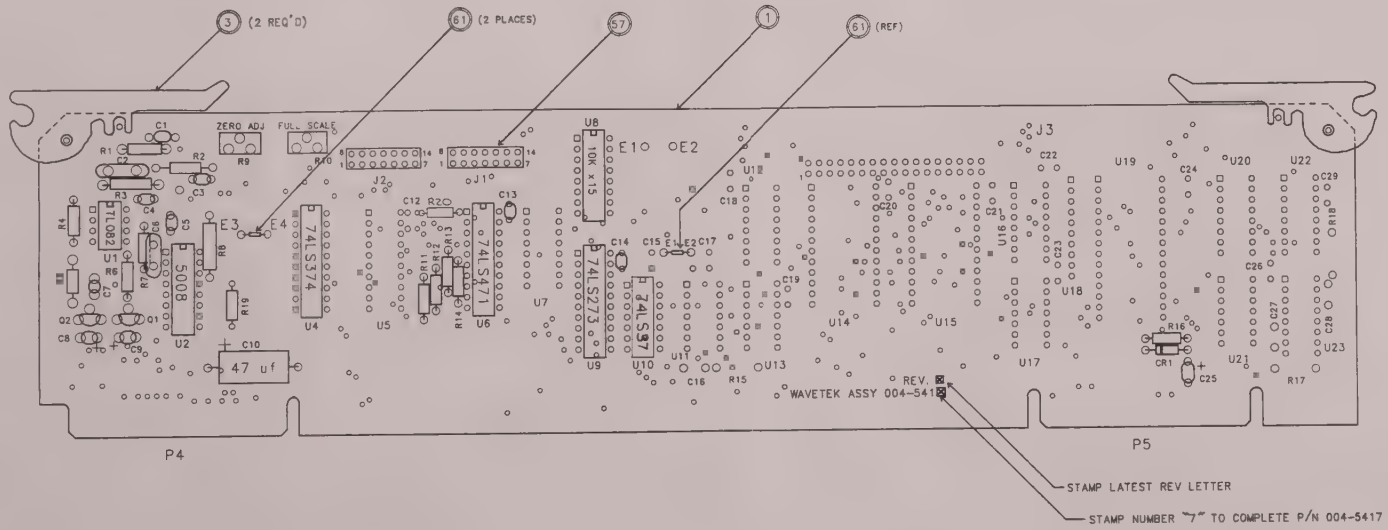
REASON EXCEPT CALIBRATION, OPERATION,
AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPRD BY		DATE
	A	RELEASE		R W	D S	10/4/84
	B	1920	N P 11/28/84	R W	S R	11/29/84
	C	2020	S R 9/27/84	S R		9/27/85
	D	2049	N P 10/29/85	D S		10/30/85
	E	2072	N P 12/10/85			
	F	205	[illegible]			
	G	205	[illegible]			



SHEETS 2 ~~AND 3 ARE~~ IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: X/X ±1/64, .XXX ±.005, .XX ±.01, ∠ ±1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.
MATERIAL: //	DRAWN N. PETERS 8/13/84	TITLE: P.W.B. ASSEMBLY BCD AMPL CONTROL
FINISH: //	CHKD SAM RAUCH	
	ENG APPR. R.W 10/2/84	
	MFG APPR	SIZE D · MODEL NO 5156A · DRAWING NO. 02-004-5417 · REV G
	ISSUED	SCALE 2:1 · 23338 · SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5417 REV G

PC ASSY: BCD AMPLITUDE,REMOTE (5156A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: IEEE INTERFACE, REM, 5150	320.5416	1.00
3	-	EJECTOR: PC, 5830	364.0404	2.00
4	U1,	U: DL LIN BIFET OP-AMP (TL082C	120.2082	1.00
5	U4	U: OCT D-FLIP 3-ST (74LS374)	125.0140	1.00
7	U10	U: QUAD 2 IN NAND BUFFER	125.7437	1.00
9	U9	U: OCT D-FLIP W/CLR (74LS273)	125.0139	1.00
11	U6	PROM: PGMD U6-5416 (129.3012)	021.1025	1.00
13	U2	DAC: 8 BIT BINARY	129.1505	1.00
15	Q1	Q: P.V. REG 5V (78L05)	120.0053	1.00
19	CR1	CR: SL LW LK 70PIV 200MW 1N457	132.0457	1.00
21	C2,C6	C: FX MICA DP 100PF +-5% 500V	101.1100	2.00
23	C5	C: FX MONO .01UF +80 -20% 50V	100.3105	1.00
25	C1,C3,C4,C7,C13,C14	C: FX MONO 0.1UF Z5U 50V	100.4102	6.00
27	C8,C9,C25	C: FX TANT 10UF 20% 20V	109.6100	3.00
29	C10	C: FX ELECT 47UF 20% 63V	109.6470	1.00
33	R10	R: VAR CMT 2.0K 3/8SQ EM	118.2203	1.00
35	R9	R: VAR CMT 10K 3/8SQ EM	118.3103	1.00
39	R5,R6,R19	R: FX MFLM 1.00K 1% 1/10W T2	111.1001	3.00
41	R11,R12,R13,R14,R20	R: FX CFLM 10K OHM 5% 1/4W	116.3101	5.00
43	R3	R: FX MFLM 2.72K 1% 1/8W T0	111.2720	1.00
45	R4,R7	R: FX MFLM 10.0K 1% 1/10W T2	112.1001	2.00
47	R2	R: FX MFLM 3.92K 1% 1/10W T2	111.3921	1.00
49	R8	R: FX MFLM 5.31K 1% 1/8W T0	111.5310	1.00
51	R16	R: FX CFLM 27K OHM 5% 1/4W	116.3271	1.00
57	J1	CONN: TERM 4 PIN SIL ST	354.0037	1.00
59	U8	U: PULL UP NET 10K 2% X15	128.3101	1.00
61	6" FOR E3-E4,E5,E6	WIRE: BUSS TINNED #22GA	378.0601	1.00
62	R1	R: FX MFLM 25.5K 1% 1/10W T2	112.2551	1.00

SECTION 7
FREQUENCY GENERATOR CIRCUITS

7.1 INTRODUCTION

The SGA and SGB modules use arithmetic operations to produce seven standard frequencies required throughout the instrument. In addition, the SGA module produces another frequency (33 MHz) used only as an input to the SGB module. The SGA module must be driven by a 5 or 10 MHz signal originating from an external source (option 000) or by an internal crystal oscillator (options 001, 002, or 004). In the case of option 000, a 10 MHz crystal filter circuit in the SGA module will double a 5 MHz input or amplify a 10 MHz input frequency to become the 10 MHz reference source for all standard internal frequencies. The SGA module drives the SGB module, and together, they produce signals coherent with the 10 MHz crystal controlled circuit that are used throughout the synthesizer. The SGA module also provides the 10 MHz input for the 10 MHz isolation amplifier that drives the 10 MHz OUT connector on the rear panel.

DC power is supplied to the SGA and SGB modules by +5.4 and −12.6 V supplies. Since the SGA and SGB outputs are constant and not subject to selection or control, no programming inputs are needed. All inputs and outputs are fed through card-edge connectors with multiple grounds to reduce internal radiation of the RF signals.

The SGA and SGB modules are unique and cannot be interchanged with any other module in the synthesizer. Both units are housed in a frame and U-cover enclosure and plug into three ten-pin connectors with asymmetric spacing to assure proper orientation. They can be removed as complete units after releasing three screws (for each module) located at the bottom of the deck.

7.2 THEORY OF OPERATION

7.2.1 Standard Crystal Oscillator (Option 002)

Option 002 is a temperature compensated crystal oscillator operating at 10.000000 MHz. It provides a typical output of 0.5 Vrms into 50 ohms. Temperature compensation is derived from the use of selected temperature sensitive components in the frequency determining circuits.

7.2.2 Standard Generator A

The SGA module produces frequencies of 18, 20, 22 and 33 MHz, each on separate outputs. It also produces all harmonics of 10 MHz from 10 to 140 MHz (picket fence) on a single output. These frequencies are used by the SGB, DM and DMA modules.

For each of the four standard frequencies produced by the SGA module (18, 20, 22 and 33 MHz), an amplifier/filter circuit selects one of the picket fence frequencies. The selected signal is then modified by the appropriate combination of addition, division and multiplication. Unwanted products of these arithmetic operations are filtered out. One of these standard frequencies (33 MHz) is used only in the SGB module to help produce the 113 MHz standard frequency.

Refer to figure 7-1 and schematic 03-004-5640. A 5 or 10 MHz input signal is applied to J21 pin 51. This signal is amplified (if a 10 MHz signal) or multiplied (if a 5 MHz signal) by Q7. At the output of Q7, a 10 MHz narrow band single-pole crystal filter (Y1 and associated components) removes noise and attenuates the 5 MHz input (if used). The resulting 10 MHz signal is buffered by emitter-follower Q6 before exiting the board at J21 pin 49. This signal is input to the DB1 module, the PLL/VCO module, and through L3 on the main board, to a 10 MHz amplifier (see paragraph 7.2.4).

Internally, this 10 MHz signal is applied to pulse generator Q4/Q5 which produces a spectrum of harmonics from 10 to 140 MHz at 10 MHz increments ("picket fence" or "10 MHz comb") at the junction of R23 and R24. The picket fence frequencies are the source of all standard frequencies in the instrument.

To produce the 22 MHz standard frequency and the 33 MHz signal used in the SGB module, transistor Q1, which is loosely coupled by C4, amplifies the picket fence signal. Tuned circuit L14, C5 and C6 allows only the 110 MHz frequency to reach digital divider U1. This circuit provides divide by five and divide by 10 outputs of 22 MHz at pin 4 and 11 MHz at pin 15 respectively. The signal at pin 4 passes through a tuned circuit (L8 and C46) where it becomes a low impedance output to the 22 MHz bus. The 11 MHz signal at pin 15 passes through tuned

circuit L6, C48, C49 and C51 which selects the third harmonic, producing a 33 MHz signal that is output only to the SGB module.

Production of the 18 MHz standard frequency is begun when C11 loosely couples the picket fence signal to transistor Q2. The 90 MHz portion of the picket fence is passed by tuned circuit L15, C12 and C13 to U2, a digital divide by five circuit. The 18 MHz output at U2 pin 4 passes through tuned circuit L10 and C42 where it becomes a low impedance 18 MHz output.

To produce the 20 MHz standard frequency, transistor Q3, which is loosely coupled by C16, amplifies the picket fence signal. The 100 MHz portion of the picket fence is passed by tuned circuit L16, C17 and C18 to U3. The 20 MHz output at U3 pin 4 passes through tuned circuit L12 and C36, providing a low impedance output.

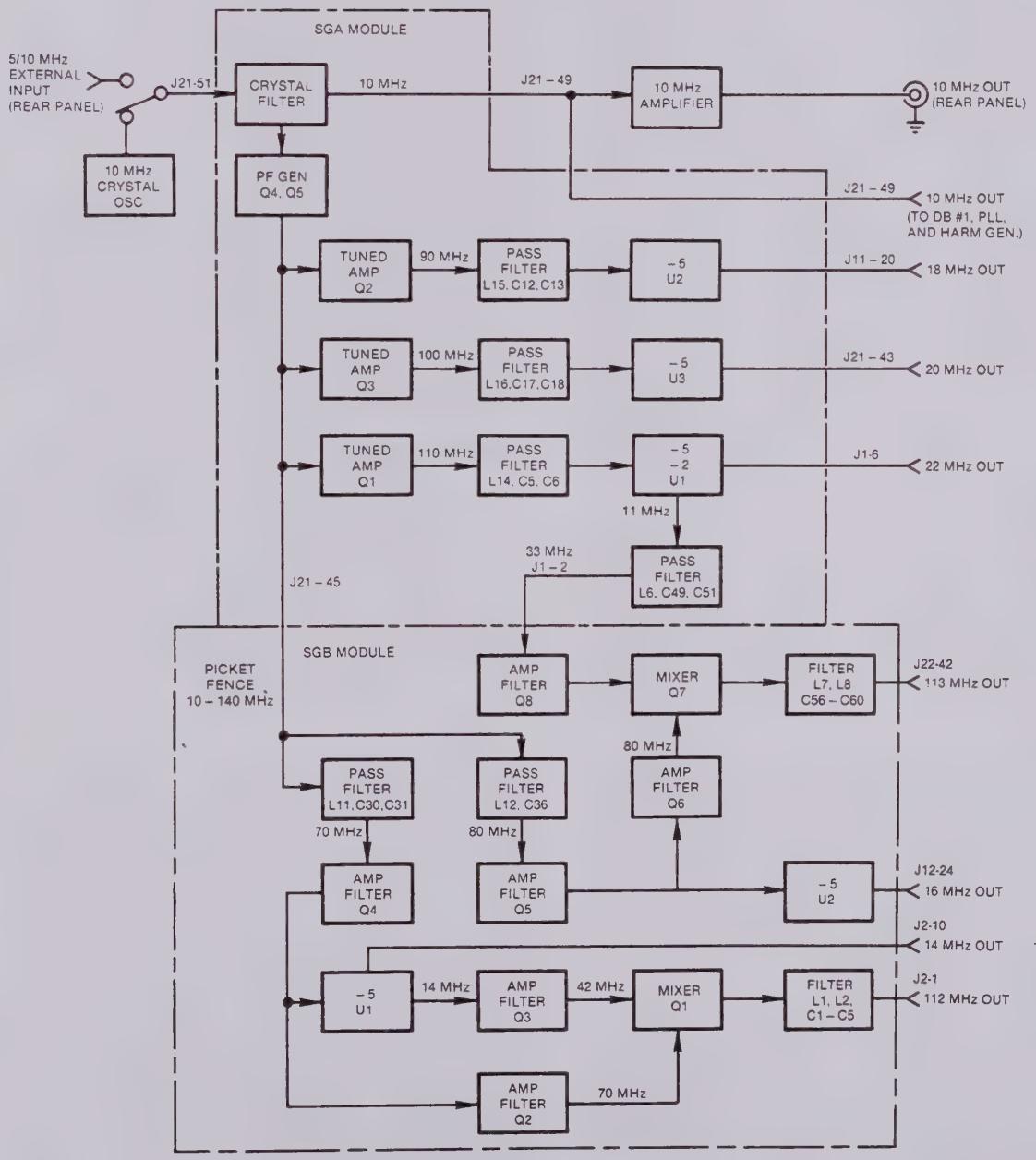


Figure 7-1. SGA and SGB Block Diagrams

7.2.3 Standard Generator B

The SGB module receives both the 33 MHz output signal and the 10 to 140 MHz picket fence from the SGA module. It produces 14, 16, 112 and 113 MHz signals, each on separate outputs. These frequencies are used by the DM and DMA modules.

For each of the four standard frequencies produced by the SGB module (14, 16, 112 and 113 MHz), an amplifier/filter circuit selects one of the picket fence frequencies. The selected signal is then modified by the appropriate combination of addition, division and multiplication. Unwanted products of these arithmetic operations are filtered out.

Refer to figure 7-1 and schematic 03-004-5645. The SGB module receives the 10 to 140 MHz picket fence at pin 20, and the 33 MHz signal at pin 47. Frequencies generated on the left half of the SGB schematic (14 MHz and 112 MHz), are derived from the 70 MHz portion of the picket fence. Frequencies generated on the right half of the SGB schematic (16 MHz and 113 MHz) are derived from the 80 MHz portion of the picket fence.

Both the 70 MHz and 80 MHz lines are pre-filtered, allowing only those frequencies to pass. The 70 MHz signal is amplified by Q4 and Q2, while the 80 MHz signal is amplified by Q5 and Q6.

U1 divides the 70 MHz signal by 5, producing 14 MHz. The third harmonic of this 14 MHz signal is supplied to amplifier Q3 from U1 pin 2. The 70 MHz signal from Q2 and the 42 MHz signal from Q3 are added in mixer Q1 to produce the 112 MHz output frequency at pin 1 of the board connector. 14 MHz is taken from U1 pin 4 for the output at pin 10.

As seen on the right side of the SGB schematic, U2 divides the 80 MHz output of amplifier Q5 by 5 to produce 16 MHz at pin 24. The 33 MHz signal from the SGA module is amplified by Q8, then added by mixer Q7 to the 80 MHz output of Q6, producing the 113 MHz signal at pin 42. Double-tuned filters are used to filter the 112 and 113 MHz mixer outputs, while single-tuned filters are used for the 14 and 16 MHz outputs.

7.2.4 10 MHz Amplifier

The 10 MHz signal at L3 on the main board is input to the 10 MHz amplifier (02-002-5467). This circuit can be used to externally drive other instruments through J5, the 10 MHz OUT rear panel connector.

7.3 SPECIFICATIONS

7.3.1 Standard Crystal Oscillator

The standard stability crystal oscillator, Option 002, has the following specifications:

Operating Frequency	10.000000 MHz.
Aging	$\pm 4 \times 10^{-6}$ per year.
Output Voltage	0.5 Vrms into 300 ohms.
Temperature Stability	$\pm 1 \times 10^{-6}$ between 0° to 50°C.
DC Supply	−12.4V @ 20 mA.

7.3.2 Standard Generator A

Input Signal	5/10 MHz (internal or external).
Output Signals	18, 20, 22, and 33 MHz. 10 to 140 MHz picket fence.
DC Supply	−12.4V at 25 mA. +5.4V at 290 mA.
Connectors	Three 10-pin edgecard.

7.3.3 Standard Generator B

Input Signals	33 MHz. 10 to 140 MHz picket fence.
Output Signals	14, 16, 112, and 113 MHz.
DC Supply	+5.4V at 195 mA. −12.4V at 54 mA.
Connectors	Three 10-pin edgecard.

7.3.4 10 MHz Amplifier

Input Frequency	10.000000 MHz.
Output Frequency	10.000000 MHz.
Gain	8 dB
DC Supply	+6.0V at 65 mA.
Connector	One panel mount BNC female.

7.4 MAINTENANCE

7.4.1 Preventive Maintenance

Preventive maintenance is not required for the crystal oscillator, SGA, SGB, or 10 MHz Amplifier modules. Normal operation is indicated by the presence of correct outputs.

All of the SGA and SGB module outputs, with the exception of the 112 and 113 MHz signals, are produced directly by integrated circuit dividers.

7.4.2 Alignment/Calibration

Refer to section 5 for alignment of the 10 MHz Amplifier module.

Field or customer alignment of the SGA and SGB modules is not advised. If realignment is required, return the assemblies to the factory for service.

7.4.3 Troubleshooting

Chapter 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If the 10 MHz amplifier or crystal oscillator modules have been isolated as the source of the problem, the only authorized service is exchange and factory repair of the module.

Replacement of a faulty crystal oscillator module requires careful use of printed circuit repair techniques.

If the SGA or SGB module has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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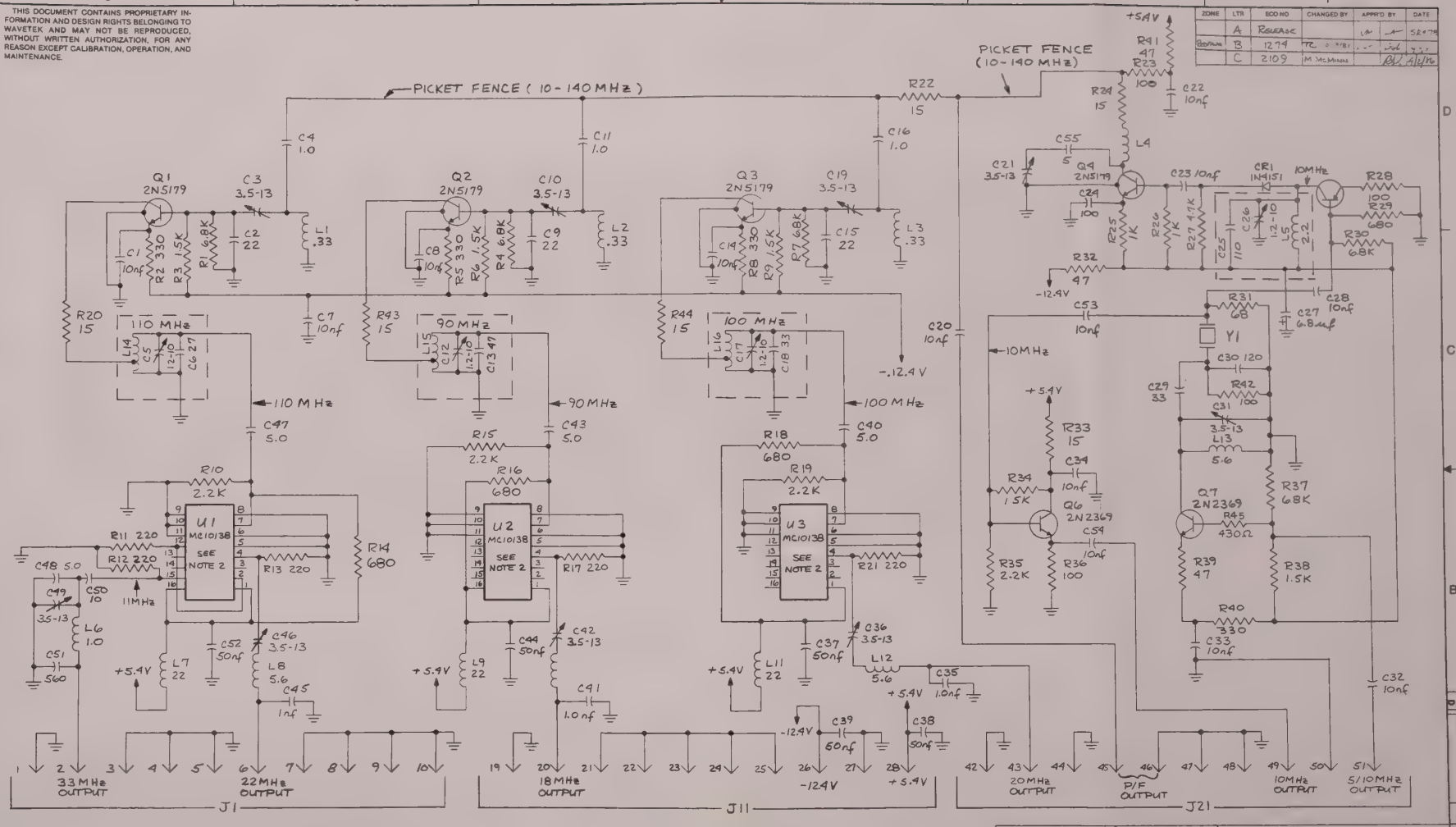
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	1279			
	C	2109	M McMANUS		4/4/86



NOTES

1) UNLESS OTHERWISE SPECIFIED:
- ALL RESISTORS ARE IN OHMS, 1/4 W, ±5%.
- ALL CAPACITORS ARE IN PF.
- ALL INDUCTORS ARE, IF SPECIFIED, IN UH.

2) TYP FOR MC10138

9	R	VEE	8
10	S1	C2	7
11	S0	S2	6
12	C1	S3	5
13	Q1	Q2	4
14	Q0	Q3	3
15	Q0	Q3	2
16	VCC2	VCC1	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: .XX ± .01, .XXX ± .005, FRACT ± 1/64, ANGLES ± 1°. MATERIAL. FINISH. DO NOT SCALE DWG. REMOVE ALL BURRS BREAK SHARP EDGES.

DRAWN — DATE 10/13/81
CHKD
ENG APPR
MFG APPR
ISSUED

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: ELECTRICAL SCHEMATIC SGA MODULE

SIZE D | MODEL NO. 5130/20 | DRAWING NO. 03-004-5640 | REV C | SCALE — | CODE IDENT 23338 | SHEET 1 OF 1

7-9/7-10

LTR	ECO NO	CHANGED BY	APPV'D BY	DATE
A	NEW RELEASE			
B	946	M McMINN		9-6-83
C	1603	MP 4/4/83		4-4-83
D	1752	[illegible]		[illegible]
E	1819	[illegible]		[illegible]
F	2043	M.McMINN		5/14/84
G	2109	M. McMINN		4/6/86

SOLDER CAP TO GND PLANE FOR C9 C10 C17 C24

SOLDER TO GND PLANE (2 PLACES)

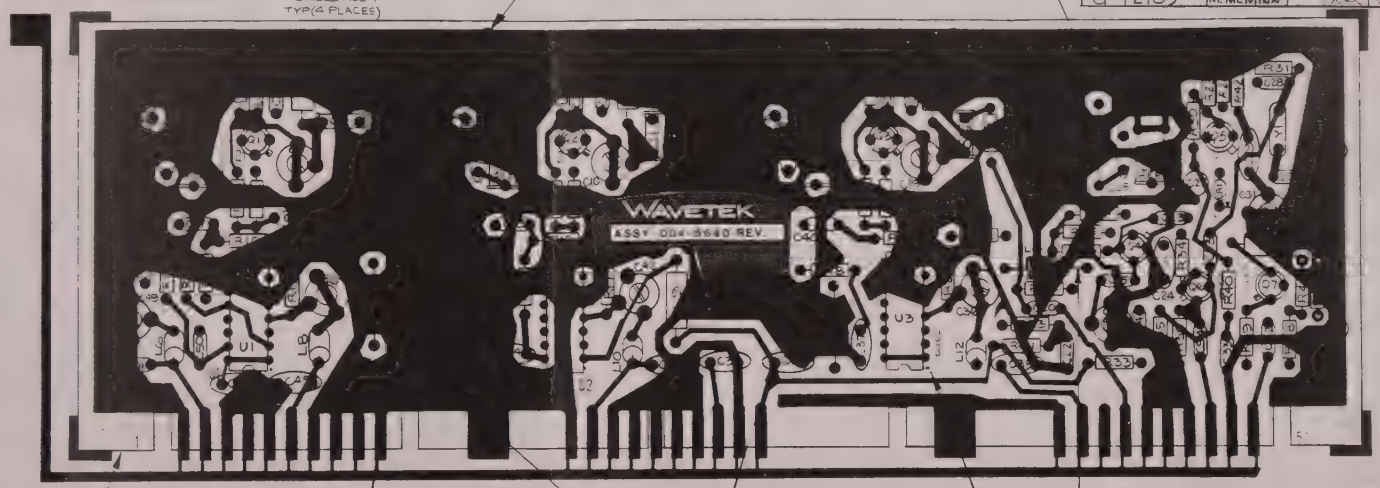
PRESS SHIELD ASS'Y TIGHTLY TO BOARD, BEND PINS OVER AND SOLDER THEM TO GND PLANE (8 PLACES)

(5) T.C. ASSY (TYP 3 PLACES) (L14, L15, L16)

(13) SHIELD ASS'Y TYP (4 PLACES)

(7) 2 REQ'D SWAGE OVER (NEARSIDE)

DONE AT THE SOLDER TAB CORNERS OF COVERS AS SHOWN (8 PLACES)



SEE NOTE 1

SEE NOTE 5

PIN 1 (TYP)

CEMENT L4 TO PC BOARD WITH Q-MAX, RF LACQUER (NOA-27 BY MULTI-TECH INDUSTRIES OR EQUIVALENT)

(1)

(11) 6 REQ'D SWAGE OVER (FARSIDE)

L6, L8, L10, L12 MOUNTED IN UPRIGHT POS

θ = 60 DEGREES (±5 DEGREES)

4-TAP SOLDERING

1/16

FIG 1

"R"

NOTES:

1. REF PT TAP: (NO SLACK IN WIRE OF TAPS)
   L14 AT 1.5 TURNS WITH R20
   L15 AT 1.5 TURNS WITH R43
   L16 AT 1.5 TURNS WITH R44
   TOLERANCE ON TAPS = ± 1/32"
2. NUMBER OF TURNS AND TAP REFRENCE POINT: "R" THE '90 O'CLOCK' POSITION ON THE COIL NEAR THE ADJUST END OF THE TRIMMER CAPACITOR AS SHOWN IN FIG NO. 1.
3. MOUNT ALL TRANSISTORS DOWN AS FAR AS POSSIBLE NOT HIGHER THEN 1/4" OFF THE BOARD.

1/32"

NOTE 5
REMOVE DUREZ FROM CAPACITOR LEADS TO 1/32" FROM BODIES MARKED WITH AN ASTERIST (*) C37, C38, C39 C44, C52.

SHEETS 2, 3 & 4 ARE "A" SIZE P/L

DRAWN BY J. JUAREZ	DATE 8-31-87	ROCKLAND Rockland Systems Corporation
CHECKED BY [illegible]	9-14-87	Confidential property of ROCKLAND SYSTEMS CORP. not to be disclosed to others, reproduced or used for any purpose except as authorized in writing by above.
ENG APPVL [illegible]	9-29-87	
MFG APPVL. [illegible]	10-14-87	

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE
.XXX ± .005
.XX ± .01
X/16 ± 1/64
∠° ± 1°

TITLE
P.C. ASSY
SGA MODULE

SIZE	DRAWING NO	REV
C	02 004-5640	G

SCALE 2:1 SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5640 REV G

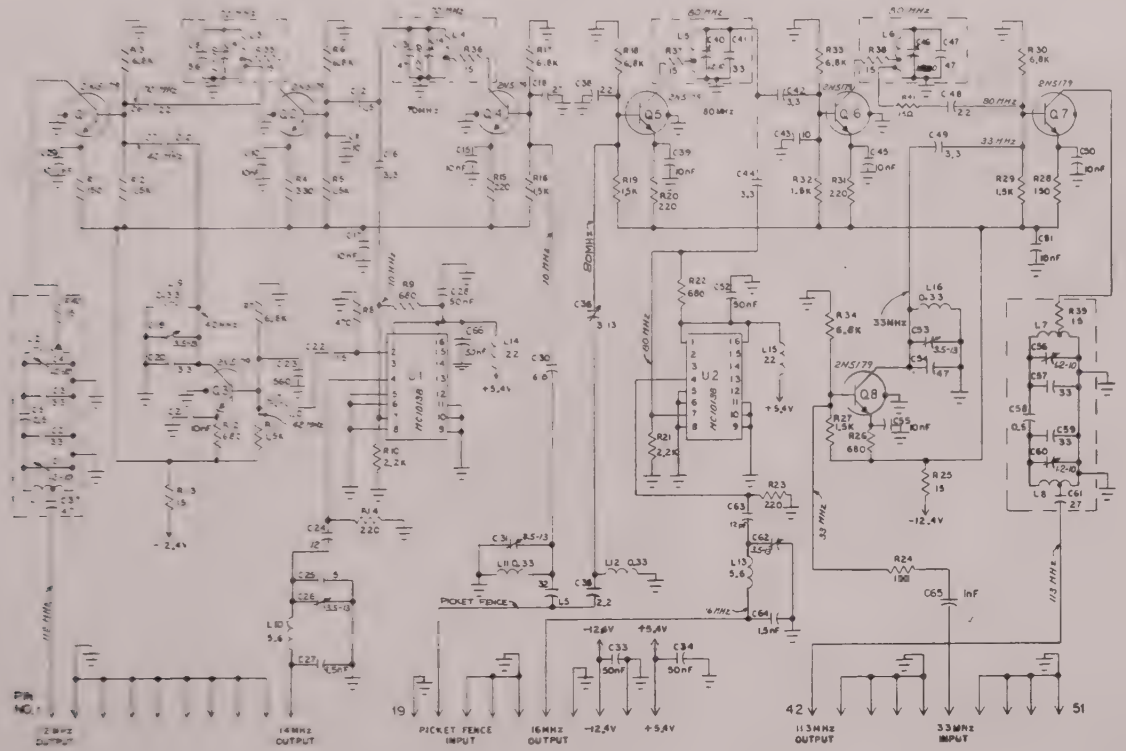
PC ASSY: SGA

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: "SGA" MODULE 5600	320.5640	1.00
5	[L14,C5] [L15,C12][L16,C17]	TUNED CKT ASSY: 5600	012.7403	3.00
7	-	SPR: THD .156D 2-56 X 3/8 SWG	389.2022	2.00
9	Y1	FILTER: CRYSTAL 10MHZ	165.3005	1.00
11	-	SPR: THD .156D 2-56 X 3/16 SWG	389.2021	6.00
13	-	SHIELD ASSY: 5600	012.6201	4.00
19	U1,U2,U3	U: BI-QUINARY CNTR (MC10138)	127.0138	3.00
24	CR1	CR: SL CMPTR 75PIV (1N4151)	132.4151	1.00
28	Q1,Q2,Q3,Q4	Q: SIL NPN (2N5179)	134.5179	4.00
29	Q5	Q: SIL PNP (2N3250)	136.3250	1.00
30	Q6,Q7	Q: SIL NPN (2N2369)	134.2369	2.00
34	R1,R4,R7,R30,R37	R: FX CFLM 6.8K OHM 5% 1/4W	116.2681	5.00
35	R2,R5,R8,R40	R: FX CFLM 330 OHM 5% 1/4W	116.1331	4.00
36	R3,R6,R9,R34,R38	R: FX CFLM 1.5K OHM 5% 1/4W	116.2151	5.00
37	R10,R15,R19,R35	R: FX CFLM 2.2K OHM 5% 1/4W	116.2221	4.00
38	R11,R12,R13,R17,R21	R: FX CFLM 220 OHM 5% 1/4W	116.1221	5.00
39	R14,R16,R18,R29	R: FX CFLM 680 OHM 5% 1/4W	116.1681	4.00
40	R20,R22,R24,R33,R43,R44	R: FX CFLM 15 OHM 5% 1/4W	116.0151	6.00
41	R23,R28,R36,R42	R: FX CFLM 100 OHM 5% 1/4W	116.1101	4.00
42	R25,R26	R: FX CFLM 1.0K OHM 5% 1/4W	116.2101	2.00
43	R27	R: FX CFLM 4.7K OHM 5% 1/4W	116.2471	1.00
44	R32,R39,R41	R: FX CFLM 47 OHM 5% 1/4W	116.0471	3.00
45	R31	R: FX CFLM 68 OHM 5% 1/4W	116.0681	1.00
46	R45	R: FX CFLM 430 OHM 5% 1/4W	116.1431	1.00
51	L1,L2,L3	L: FXD .33 UHY +/-20%	150.8332	3.00
52	L4	L: AIR IND .20UH NOM	012.1002	1.00
53	L6	L: FXD 1.0 UHY +/-10%	150.9102	1.00
54	L7,L9,L11	L: FXD 22 UHY +/-20%	150.8222	3.00
55	L8,L10,L12,L13	L: FXD 5.6 UHY +/-10%	150.9562	4.00
56	L5	L: FXD 2.2 UHY +/-10%	150.9222	1.00
60	C1,C7,C8,C14,C20,C22,C23,	C: FX CER .01UF +80 -20% 50V	100.3101	13.00
60	C28,C32,C33,C34,C53,C54	C: FX CER .01UF +80 -20% 50V	100.3101	0.00
62	C2,C9,C15	C: FX CER 22PF 5% NPO 500V	100.0229	3.00
63	C46,C49	C: VAR CER 3.5-13PF 5% 500V	108.0130	0.00
63	C3,C10,C19,C21,C31,C36,C42	C: VAR CER 3.5-13PF 5% 500V	108.0130	9.00
64	C4,C11,C16	C: FX CRM TUB 1.0PF .25PF NPO	106.9109	3.00
65	C6	C: FX CER 27PF 5% NPO 500V	100.0279	1.00
66	C13	C: FX CER 47PF 5% NPO 500V	100.0479	1.00
67	C18,C29	C: FX CER 33PF 5% NPO 500V	100.0339	2.00
68	C24	C: FX CER 100PF 10% X5F 500V	100.1105	1.00
69	C27	C: FX TANT 6.8UF 20% 16V	109.5680	1.00

WAVETEK SD INC. DWG NO. 02 004 5640 REV G

PC ASSY: SGA

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
70	C30	C: FX CER 120PF 10% X5F 500V	100.1125	1.00
71	C35,C41,C45	C: FX CER .001UF 10% X5F 500V	100.2105	3.00
72	C37,C38,C39,C44,C52	C: FX CER .05UF 20% Y5P 25V	100.3501	5.00
73	C40,C43,C47,C48,C55	C: FX CER 5.0PF .25PF NPO 500V	100.9509	5.00
74	C50	C: FX CER 10PF 5% NPO 500V	100.0109	1.00
75	C51	C: FX CER 560PF 10% X5F 500V	100.1565	1.00
76	C25	C: FX MICA DP 110PF +-5% 500V	101.1110	1.00
77	C26	C: VAR CER 1.2-10PF 5% 500V	108.0100	1.00



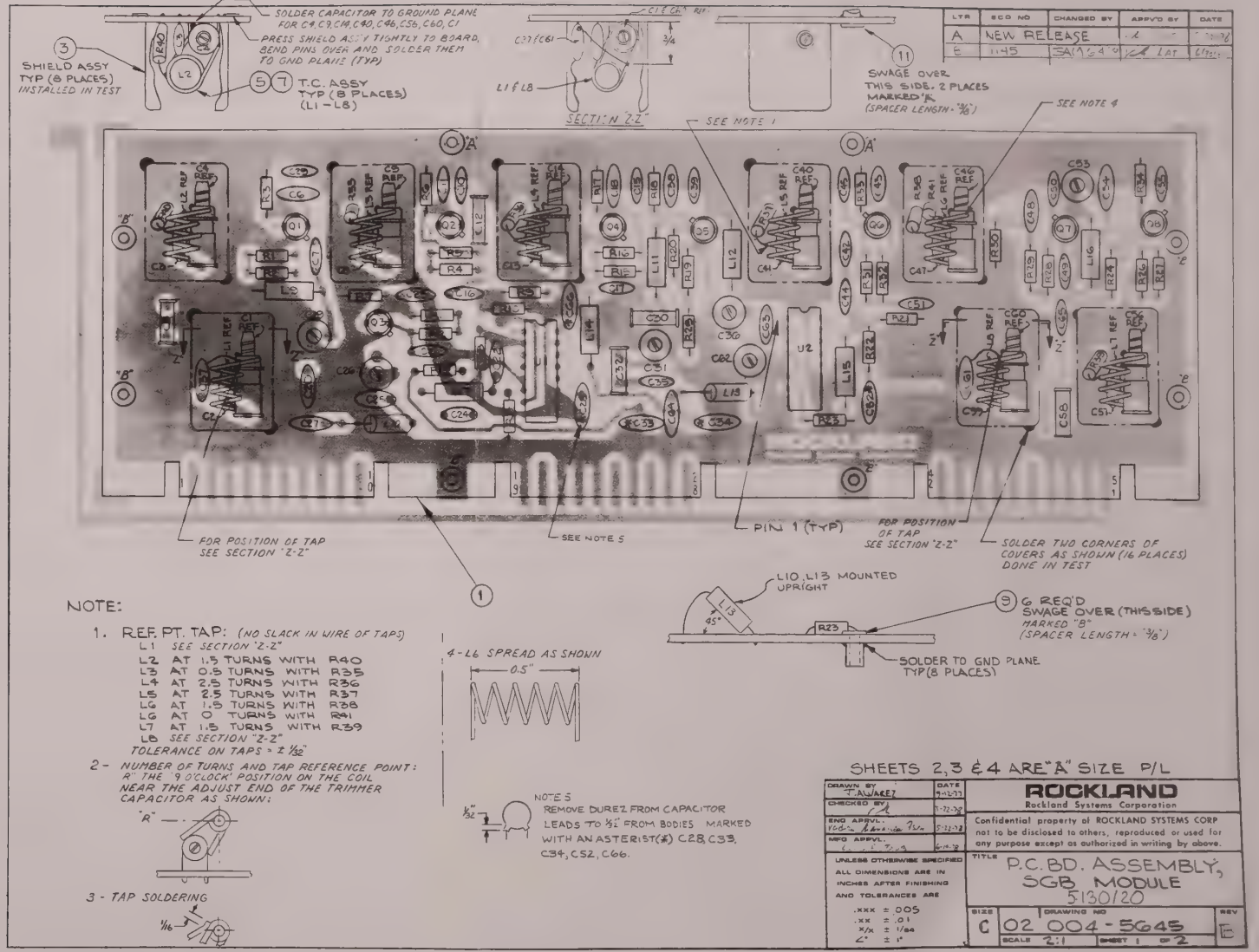
NOTE:
1-UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS 1/4 W ± 5%, ALL CAPACITORS ARE IN PF, ALL INDUCTORS IF SPECIFIED ARE IN UH

LTR	ECO NO	CHANGED BY	APPD BY	DATE
B	329			

DRAWN BY M McMinn	DATE 1-4-77	ROCKLAND Rockland Systems Corporation
CHECKED BY	1-11-77	
ENGR APPVL		Confidential property of ROCKLAND SYSTEMS CORP not to be disclosed to others, reproduced or used for any purpose except as authorized in writing by above.
MFG APPVL		
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER PLATING AND TOLERANCES ARE .XXX ± — .XX ± — X/32 ± 1/64 ∠° ± 1°		TITLE SCHEMATIC, SGB, MODULE
		SIZE D DRAWING NO. 03-004-5645 REV B
		SCALE N/C SHEET 1 OF 1

03-004-5645 REV B

7-17/7-18


SOLDER CAPACITOR TO GROUND PLANE FOR C4,C9,C19,C40,C46,C56,C60,C1
PRESS SHIELD ASSY TIGHTLY TO BOARD, BEND PINS OVER AND SOLDER THEM TO GND PLANE (TYP)
3 SHIELD ASSY TYP (8 PLACES) INSTALLED IN TEST
5 7 T.C. ASSY TYP (8 PLACES) (L1 - L8)
SECTION Z-Z
11 SWAGE OVER THIS SIDE. 2 PLACES MARKED 'A' (SPACER LENGTH = 3/8)
SEE NOTE 1
SEE NOTE 4
FOR POSITION OF TAP SEE SECTION "Z-Z"
SEE NOTE 5
PIN 1 (TYP)
FOR POSITION OF TAP SEE SECTION "Z-Z"
SOLDER TWO CORNERS OF COVERS AS SHOWN (16 PLACES) DONE IN TEST
1
L10, L13 MOUNTED UPRIGHT
9 6 REQ'D SWAGE OVER (THIS SIDE) MARKED "B" (SPACER LENGTH = 3/8")
SOLDER TO GND PLANE. TYP (8 PLACES)

LTR	ECO NO	CHANGED BY	APPV'D BY	DATE
A	NEW RELEASE			
E	1145	SA	LAT	

NOTE:

1. REF. PT. TAP: (NO SLACK IN WIRE OF TAPS)
   - L1 SEE SECTION "Z-Z"
   - L2 AT 1.5 TURNS WITH R40
   - L3 AT 0.5 TURNS WITH R35
   - L4 AT 2.5 TURNS WITH R36
   - L5 AT 2.5 TURNS WITH R37
   - L6 AT 1.5 TURNS WITH R38
   - L6 AT 0 TURNS WITH R41
   - L7 AT 1.5 TURNS WITH R39
   - L8 SEE SECTION "Z-Z"

   TOLERANCE ON TAPS = ± 1/32"
2. NUMBER OF TURNS AND TAP REFERENCE POINT: R" THE "9 O'CLOCK" POSITION ON THE COIL NEAR THE ADJUST END OF THE TRIMMER CAPACITOR AS SHOWN:

3 - TAP SOLDERING

4 - L6 SPREAD AS SHOWN

NOTE 5
REMOVE DUREZ FROM CAPACITOR LEADS TO 1/32" FROM BODIES MARKED WITH AN ASTERIST(*) C28, C33, C34, C52, C66.

SHEETS 2, 3 & 4 ARE "A" SIZE P/L

DRAWN BY: T.A. WACEK	DATE: 9-12-77
CHECKED BY:	9-22-78
ENG APPVL:	9-22-78
MFG APPVL:	9-14-78

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE
.XXX ± .005
.XX ± .01
X/x ± 1/64
∠° ± 1°

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TITLE: P.C. BD. ASSEMBLY, SGB MODULE 5130120

SIZE	DRAWING NO	REV
C	02 004-5645	E
SCALE 2:1	SHEET 1 OF 2	

WAVETEK SD INC. DWG NO. 02 004 5645 REV B

PC ASSY: SGB

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: "SGB" MODULE 5600	320.5645	1.00
3	-	SHIELD ASSY: 5600	012.6201	[illegible]
5	(L1,C1)(L2,C4)(L7,C56)	TUNED CKT ASSY: 5600	012.7401	4.00
5	(L8,C60)	TUNED CKT ASSY: 5600	012.7401	[illegible]
7	L3,C9)(L4,C16)(L5,C40)	TUNED CKT ASSY: 5600	012.7402	3.00
8	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8	Q: SIL NPN (2N5179)	134.5179	[illegible]
9	-	SPR: THD .156D 2-56 X 3/16 SWG	[illegible]	[illegible]
11	-	SPR: THD .156D 2-56 X 3/8 SWG	[illegible]	2.00
13	(L6,C46)	TUNED CKT ASSY: "SGB" MODULE	[illegible]	1.00
25	U1,U2	U: BI-QUINARY CNTR (MC10138)	127.0138	2.00
28	L9,L11,L12,L16	L: FXD .33 UHY +/-20%	[illegible]	4.00
29	L10,L13	L: FXD 5.6 UHY +/-10%	150.9562	2.00
30	L14,L15	L: FXD 22 UHY +/-20%	[illegible]	2.00
31	L17	L: FXD 1.0 UHY +/-10%	150.9102	1.00
34	C2,C3,C20,C41,C57,C59	C: FX CER 33PF 5% NPO 500V	[illegible]	[illegible]
35	C5,C58	C: FX CRM TUB 0.5PF .25PF NPO	[illegible]	2.00
36	C6,C38,C48	C: FX CER 22PF 5% NPO 500V	[illegible]	3.00
37	C7,C35	C: FX CER 2.2PF .5PF NPO 500V	[illegible]	[illegible]
38	[illegible]	C: FX MICA DP 56PF +-5% 500V	101.0560	1.00
39	C10,C15,C17,C21,C29,C39,C45	C: FX CER .01UF +80 -20% 50V	[illegible]	10.00
39	C50,C51,C55	C: FX CER .01UF +80 -20% 50V	100.3101	[illegible]
41	C11,C43	C: FX CER 10PF 5% NPO 500V	100.0109	2.00
42	C12,C32	C: FX CRM TUB 1.5PF .25PF NPO	106.9159	2.00
43	C13,C37,C47,C54	C: FX CER 47PF 5% NPO 500V	[illegible]	[illegible]
44	C16,C42,C44,C49	C: FX CER 3.3PF .5PF NPO 500V	100.9339	[illegible]
45	C18,C61	C: FX CER 27PF 5% NPO 500V	[illegible]	2.00
46	C19,C26,C31,C36,C53,C62	C: VAR CER 3.5-13PF 5% 500V	108.0130	6.00
47	C22	C: FX CER 15PF 5% NPO 500V	[illegible]	1.00
48	C23	C: FX CER 560PF 10% XSF 500V	100.1565	1.00
49	C25	C: FX CER 5.0PF .25PF NPO 500V	[illegible]	1.00
50	C27,C64	C: FX CER .1015UF 10% XSF 500V	100.2155	2.00
51	C28,C33,C34,C52,C66	C: FX CER .05UF +20-80 YSF 12V	[illegible]	5.00
52	C65	C: FX CER .001UF 10% XSF 500V	100.2105	1.00
53	C30	C: FX CRM TUB 6.8PF .25PF NPO	[illegible]	1.00
54	C24,C63	C: FX CER 12PF 5% NPO 500V	100.0129	2.00
61	R1,R24,R28	R: FX CFLM 150 OHM 5% 1/4W	116.1151	3.00
62	R2,R5,R11,R16,R19,R27,R29,	R: FX CFLM 1.5K OHM 5% 1/4W	116.2151	[illegible]
62	R32	R: FX CFLM 1.5K OHM 5% 1/4W	116.2151	[illegible]
63	R34	R: FX CFLM 6.8K OHM 5% 1/4W	116.2681	[illegible]
63	R3,R6,R7,R17,R18,R30,R33,	R: FX CFLM 6.8K OHM 5% 1/4W	116.2681	8.00
64	[illegible]	R: FX CFLM 330 OHM 5% 1/4W	116.1331	1.00

WAVETEK SD INC. DWG NO. 02 004 5645 REV B

PC ASSY: SGB

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
65	R8	R: FX CFLM 470 OHM 5% 1/4W	116.1471	1.00
66	R9,R12,R22,R26	R: FX CFLM 680 OHM 5% 1/4W	116.1681	4.00
67	R20,R21	R: FX CFLM 2.2K OHM 5% 1/4W	116.2221	2.00
68	R13,R25,R35 THRU R41	R: FX CFLM 15 OHM 5% 1/4W	116.0151	9.00
69	R14,R15,R20,R23,R31	R: FX CFLM 220 OHM 5% 1/4W	116.1221	5.00

SECTION 8
DIGITAL BOARDS 1 AND 2

8.1 INTRODUCTION

The DB1 and DB2 modules determine the digits for the 0.1 Hz to 10 kHz ranges. Digits for the 1 and 10 kHz ranges are set by the DB1 board, while those for ranges 0.1 through 100 Hz are determined by the DB2 board. Together, these boards control a digital to analog converter (DAC) located in the DB1 board that produces an output signal of the correct frequency.

The boards mount in a card cage each using two connectors with asymmetric spacing assuring proper orientation. They are held in place by the connectors 5and the instrument's top cover resting on the ejectors mounted on the board.

8.2 THEORY OF OPERATION

The DB1 and DB2 boards are shown in figure 8-1. The schematics for these boards are proprietary to Wavetek and therefore not included or discussed in this manual. The frequency, as programmed from either the front panel or remote connectors, enters the DB1 and DB2 boards in BCD format. Internal connections on the digital boards have the effect of multiplying this BCD frequency by 10. For example, if the programmed frequency is 14.210 kHz, the DB1 and DB2 boards will see an input of 142.100 kHz. This decimal point movement will be compensated for in the DM module by shifting all digits at or below the 100 kHz range one decade to the right.

The BCD format entered into the DB1 and DB2 boards is converted to binary, then stored in a frequency register. In the DB1 board, a 1 MHz carrier frequency is added at the frequency register to the 1 and 10 kHz (actually 10 and 100 kHz) binary input, producing a signal between 1 and 2 MHz. The output of the DB1 and DB2 frequency registers are each clocked into phase accumulators at a 10 MHz rate. The phase accumulator on the DB2 board drives a register that provides the DB1 board phase accumulator with the 0.1 to 100 Hz frequencies. The output of the DB1 phase accumulator, through a register, controls a sine table ROM that produces a sine wave sample. This is converted to analog form by a digital-to-analog converter (DAC), followed by a smoothing low pass filter (LPF) with a cut-off frequency of approximately 4 MHz.

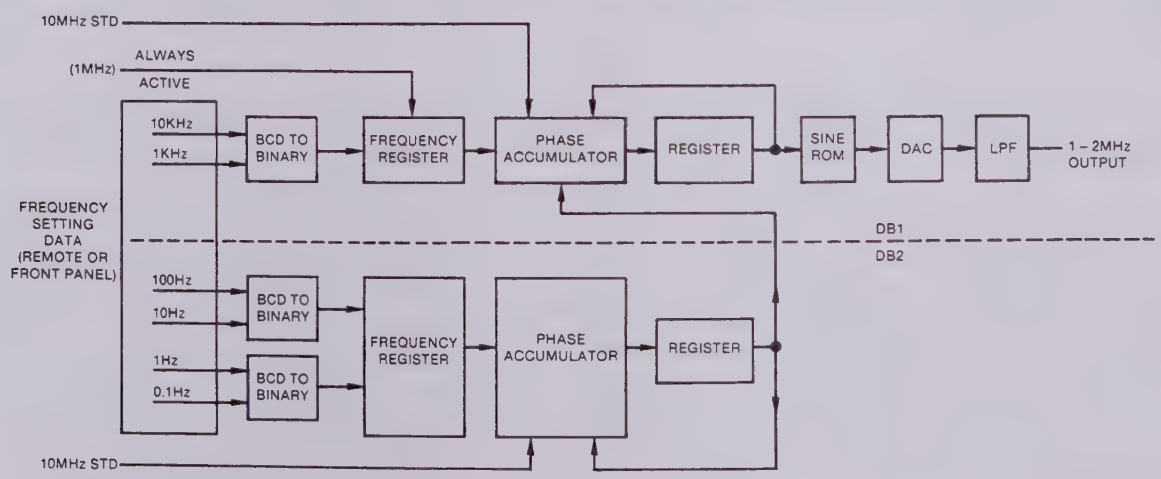


Figure 8-1 Digital Board (DB1 and DB2) Block Diagram

8.3 SPECIFICATIONS

8.3.1 Digital Board 1

The digital board 1 has the following specifications:

Programming Inputs	1, 2, 4, and 8 BCD (positive true). High = +3.0V minimum. Low = +0.5V maximum.
Output Signals	1 to 2 MHz sine waves.
Spurious Outputs	Better than −50 dB.
DC Supply	+5.4V at 665 mA. −12.4V at 25 mA. +23V at 120 mA.
Connectors	Two 30-pin edgecard. Two SMA female.

8.3.2 Digital Board 2

The digital board 2 has the following specifications:

Programming Inputs	1, 2, 4, and 8 BCD (positive true). High = +3.0V minimum. Low = +0.5V maximum.
Output Signals	Accumulator Digital Signals.
DC Supply	+5.4V at 350 mA.
Connectors	Two 30-pin edgecard.

8.4 MAINTENANCE

8.4.1 Preventive Maintenance

Preventive maintenance is not required for the DB1 or DB2 boards. Normal operation is indicated by the presence of correct outputs.

8.4.2 Alignment/Calibration

Field or customer alignment of the DB1 or DB2 boards is not advised. If realignment is required, return the assembly to the factory for service.

8.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before attempting to replace an assembly.

If the DB1 or DB2 board has been isolated as the source of the problem, the only authorized service is exchange and factory repair of the board.

SECTION 9
UPCONVERTER

9.1 INTRODUCTION

The upconverter module is used to translate the 1 to 1.999,999,9 MHz output from digital board 1 to between 14 and 14.999,999,9 MHz for use as an input to the DM module.

This module is housed in a frame and U-cover enclosure and plugs in to one ten-pin connector. It can be removed as a complete unit after releasing the screws located at the bottom of the deck.

9.2 THEORY OF OPERATION

Refer to figure 9-1. The upconverter schematic is proprietary to Wavetek and not included or discussed in detail in this manual. The filter at the input of the upconverter picks off the 130 MHz signal from the 10 MHz comb. This signal is divided by 10 to essentially become a 13 MHz local oscillator. When mixed with the 1 to 1.999,999,9 MHz signal from the DB1 board, a 14 to 14.999,999,9 MHz signal is produced. The final filter removes unwanted frequencies before reaching the output. For digits up to and including 10 kHz, the output frequency is 14 MHz for settings of all zeroes and 14.999,999,9 MHz for settings of all nines.

9.3 SPECIFICATIONS

The upconverter specifications are as follows:

Control Input Signals	1.0 to 1.999,999,9 MHz
Input Signal	10 to 140 MHz Comb
Output Signals	14.0 to 14.999,999,9 MHz
DC Supply	+5.4V at 85 mA.
	−12.4V at 130 mA.
Connectors	One 10-pin edgecard
	Two SMA female.

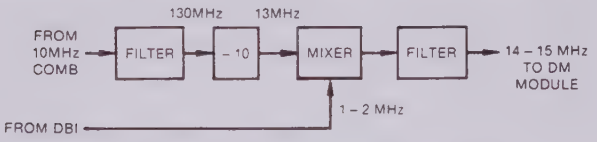


Figure 9-1. Upconverter Block Diagram

9.4 MAINTENANCE

9.4.1 Preventive Maintenance

Preventive maintenance is not required for the upconverter board. Normal operation is indicated by the presence of correct outputs.

9.4.2 Alignment/Calibration

Field or customer alignment of this assembly is not advised. If realignment is required, return the assembly to the factory for service.

9.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before attempting to replace an assembly.

If the has been isolated as the source of the problem, the only authorized service is exchange and factory repair of the module.

If the upconverter module has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

SECTION 10
DIGIT MODULE

10.1 INTRODUCTION

The digit module (DM) generates the 1 MHz digit. This module is very similar to the DMA module which it feeds. As well as containing the 100 kHz steps, the DM module output (14.000 to 14.999,999,9 MHz) also contains all the finer steps down to 0.1 Hz.

The module combines analog, VHF and digital techniques. It is programmed through card-edge connectors with multiple low-inductance grounds provided for the RF signals.

10.2 THEORY OF OPERATION

The DM module uses fixed bus signal frequencies from the SGA and SGB modules to modify the signal from the upconverter (between 14.000 and 14.999,999,9 MHz). In effect, the DM module moves each digit below the decimal point one position to the right and inserts a new digit (the 100 kHz frequency digit of the instrument as programmed from either the front panel or a remote connector) in the space provided. For example, if the DM module input signal is 14.210 MHz and the instrument 100 kHz frequency digit is 3, the output frequency of the DM module will be 14.3210 MHz. The DM output signal is used to drive the DMA module.

The fixed bus frequencies used in the DM module are 14, 16, 18, 20, 22, 112, and 113 MHz. For any 100 kHz digit selected, the DM uses either 112 MHz (for all even digits) or 113 MHz (for all odd digits) and one of the five lower frequencies, 14 MHz for digits 0 and 1, 16 MHz for digits 2 and 3, 18 MHz for digits 4 and 5, and so on.

Refer to schematic 03-004-5165. The 14.000 to 14.999,999,9 MHz signal from the upconverter (14.210 for this example) enters the DM module at J4 pin 3 where it is fed to the base of mixer Q10. The digit 1 control line, (pin 5) selects either Q1 or Q2 to direct the appropriate frequency (112 or 113 MHz respectively) to the base of Q10. Since the digit used in this example is odd (3), J4 pin 5 and U1 pin 5 are high, putting a low at U1 pin 6 and the base of Q2. With Q2 selected, Q10 mixes the 113 MHz signal from the SGB module with the 14.210 MHz signal from the upconverter. The sum of the two inputs (113 MHz plus 14.210 MHz) is 127.210 MHz.

Two 216 to 128 MHz double-tuned filters (C32 to C45 and associated components) along with amplifier Q11 select the upper sideband and filter out unwanted frequencies.

The 127.210 signal from the first mixer enters a second additive mixer consisting of Q8 and Q9. One of the switch transistors, Q3 through Q7 (Q5 for this example) provides the second input to this mixer. Since the digit used in this example is 3, J4 pin 6 is high and U2 to selects the 16 MHz signal at J4 pin 24 by placing a low at the base of Q5. Transformer T1 passes the 16 MHz output of Q5 to the second mixer where it is summed with the 127.210 MHz signal to produce 143,210 MHz. As with the previous mixer, two double-tuned filters (C46 to C59 and associated components) along with amplifier Q12 select the upper sideband (140 to 150 MHz) while suppressing the lower sideband and other unwanted frequencies.

Digital counter U3 divides the 143,210 MHz signal by ten to produce a frequency of 14.3210. A third filter (C61 to C64 and associated components) removes unwanted signals and feeds frequencies between 14 and 15 MHz to the DM module output at pin 50. Effectively, a "3" has been placed ahead of the "210" in the DM module input frequency of 14.210 MHz, producing an output frequency of 14.3210 MHz.

10.3 SPECIFICATIONS

The digit module has the following specifications:

Signal Inputs	14 to 15 MHz 14, 16, 18, 20, 22, 112 and 113 MHz.
Programming Inputs	1, 2, 4, and 8 BCD (positive true). High = +3.0V minimum. Low = +0.5V maximum.
Signal Output	14 to 15 MHz.
Spurious Outputs	Better than −70dB.
DC Supply	+6V at 100 mA (±10 mA). −12.4V at 38 mA (±3.8 mA).
Connectors	Three 10-pin edgecard.

10.4 MAINTENANCE

10.4.1 Preventive Maintenance

Preventive maintenance is not required for the digit module. Normal operation is indicated by the presence of correct outputs.

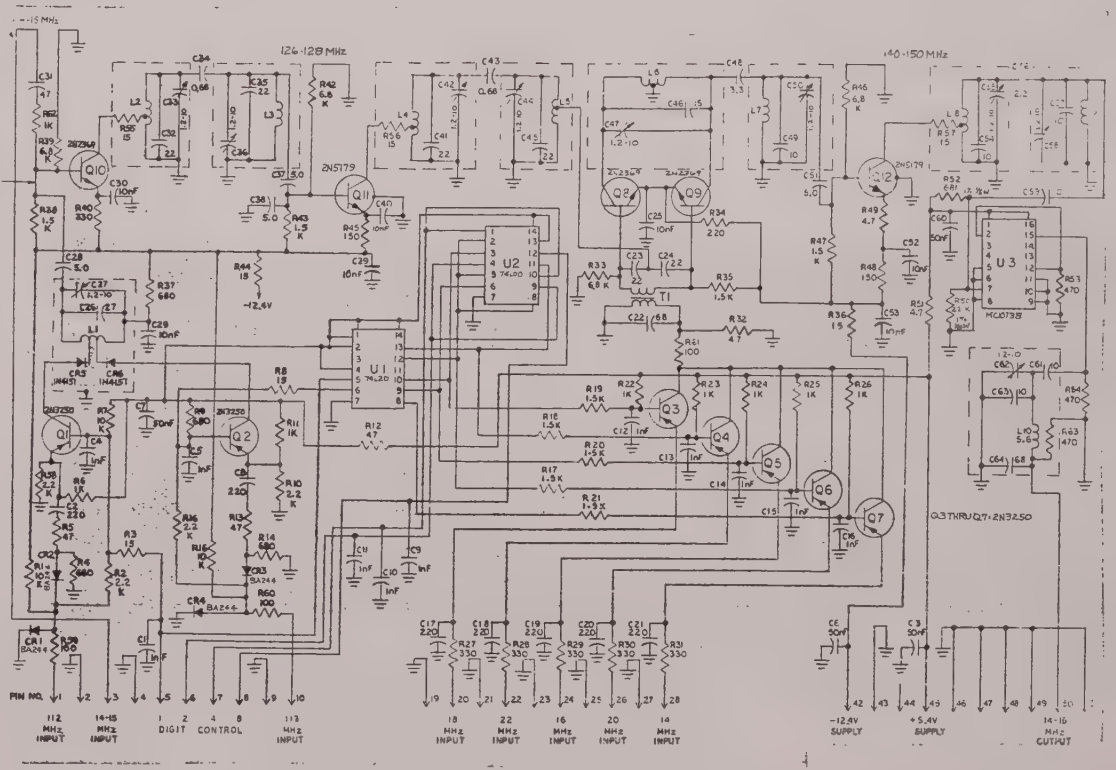
10.4.2 Alignment/Calibration

Field or customer alignment of this assembly is not advised. If realignment is required, return the assembly to the factory for service.

10.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before attempting to replace an assembly.

If the digit module has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.



NOTE:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS, ½W ± 5%. ALL CAPACITORS ARE IN PF.

LTR	ECO NO	CHANGED BY	APPV'D BY	DATE
A				

DRAWN BY		DATE
CHECKED BY		
ENG APPVL		
MFG APPVL		

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE .XXX ± — .XX ± — X/64 ± 1/64 ∠° ± 1°

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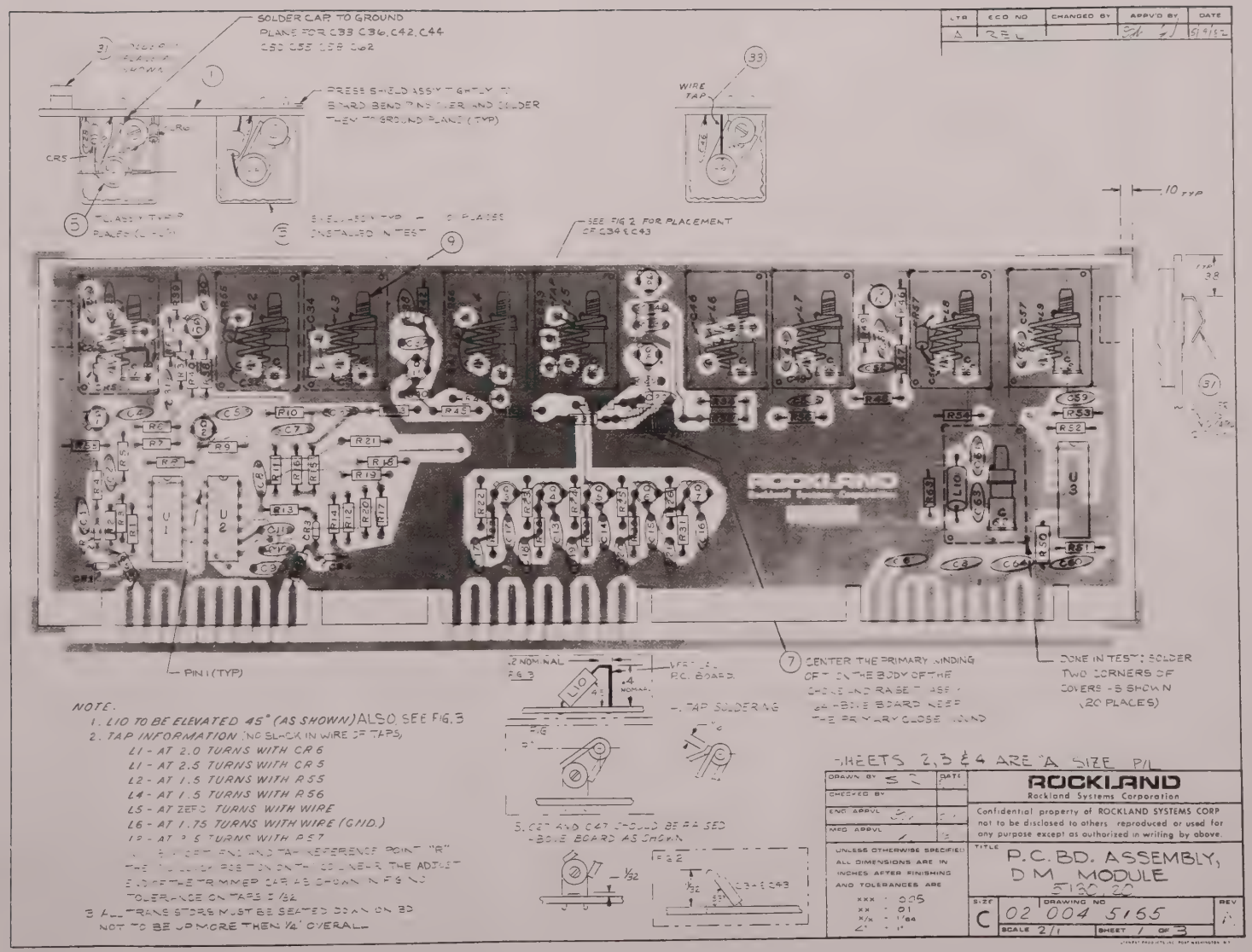
TITLE: SCHEMATIC DM MODULE

SIZE D | DRAWING NO. 03 004-5165 | REV A

SCALE — | SHEET OF


SOLDER CAP TO GROUND PLANE FOR C33 C36, C42, C44 C50 C55 C58 C62
PRESS SHIELD ASSY TIGHTLY TO BOARD BEND TABS OVER AND SOLDER THEN TO GROUND PLANE (TYP)
WIRE TAP
10 TYP
SEE FIG 2 FOR PLACEMENT OF C34 & C43
PIN 1 (TYP)
.2 NOMINAL FIG 3
.4 NOMINAL
.4
.6
1/32
1/32
5. C27 AND C47 SHOULD BE RAISED FROM BOARD AS SHOWN
7. CENTER THE PRIMARY WINDING OF T1 ON THE BODY OF THE CHOKE AND RAISE T1 ASSY FROM PC BOARD KEEP THE PRIMARY CLOSE TO BOARD
DONE IN TEST: SOLDER TWO CORNERS OF COVERS AS SHOWN (20 PLACES)
ROCKLAND

NOTE:

1. L10 TO BE ELEVATED 45° (AS SHOWN) ALSO SEE FIG. 3
2. TAP INFORMATION (NO SLACK IN WIRE OF TAPS)
   - L1 - AT 2.0 TURNS WITH CR 6
   - L1 - AT 2.5 TURNS WITH CR 5
   - L2 - AT 1.5 TURNS WITH R55
   - L4 - AT 1.5 TURNS WITH R56
   - L5 - AT ZERO TURNS WITH WIRE
   - L6 - AT 1.75 TURNS WITH WIRE (GND.)
   - T1 - AT 2.5 TURNS WITH R57
   - (4) EQUIDISTANT AND TAP REFERENCE POINT "R" THE CENTER POSITION ON THE COIL NEAR THE ADJUST END OF THE TRIMMER CAP AS SHOWN IN FIG NO TOLERANCE ON TAPS ± 1/32
3. ALL TRANSISTORS MUST BE SEATED DOWN ON BD NOT TO BE UP MORE THEN 1/4" OVERALL

SHEETS 2, 3 & 4 ARE "A" SIZE P/L

LTR	ECO NO	CHANGED BY	APPV'D BY	DATE
A	REL			5/9/62

		DATE
DRAWN BY		
CHECKED BY		
ENG APPVL		
MFG APPVL		

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE
XXX ± .005
XX ± .01
X/x ± 1/64
∠° ± 1°

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TITLE: P.C. BD. ASSEMBLY, D M MODULE 5130.20

SIZE	DRAWING NO	REV
C	02 004 5165	
	SCALE 2/1	SHEET 1 OF 3

WAVETEK SD INC. DWG NO. 02 004 5165 REV A

PC ASSY: DM

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: "DM" MODULE S600	320.5665	1.00
3	[L1-L10] INSTLD IN TEST	SHIELD ASSY: S600	012.6201	10.00
5	(L1C27)(L2C33)(L4C42)	TUNED CKT ASSY: S600	012.7401	8.00
5	(L5C44)(L6C47)(L7C50)	TUNED CKT ASSY: S600	012.7401	0.00
5	(L8C55)(L9C58)	TUNED CKT ASSY: S600	012.7401	0.00
7	T1	TRANSFORMER ASSY: S600	012.7301	1.00
9	(L3C36)	TUNED CKT ASSY: "DM" MODULE	012.7407	1.00
11	Q1,Q2,Q3,Q4,Q5,Q6,Q7	Q: SIL PNP (2N3250)	136.3250	7.00
13	Q8,Q9,Q10	Q: SIL NPN (2N2369)	134.2369	3.00
15	Q11,Q12	Q: SIL NPN (2N5179)	134.5179	2.00
19	U1	U: DUAL 4 IN NAND GATE	121.7420	1.00
21	U2	U: QUAD 2 IN NAND GATE	121.7400	1.00
23	U3	U: BI-QUINARY CNTR (MC10138)	127.0138	1.00
26	CR5 AND CR6	CR: SL CMPTR 75PIV (1N4151)	132.4151	2.00
27	CR1 THRU CR4	CR: SWITCHING (BA482 OR BA244)	133.0244	4.00
29	L10	L: FXD 5.6 UHY +/-10%	150.9562	1.00
31	-	SPRING: CONTACT, "DM" MODULE	304.0869	2.00
33	6"	WIRE: BUSS HD DWN TND #20 AWG	378.0500	0.00
34	R1,R7,R15	R: FX CFLM 10K OHM 5% 1/4W	116.3101	3.00
36	R10,R58,R2,R16	R: FX CFLM 2.2K OHM 5% 1/4W	116.2221	4.00
38	R3,R8,R36,R44,R55,R56,R57	R: FX CFLM 15 OHM 5% 1/4W	116.0151	7.00
40	R4,R9,R14,R37	R: FX CFLM 680 OHM 5% 1/4W	116.1681	4.00
42	R5,R12,R13,R32	R: FX CFLM 47 OHM 5% 1/4W	116.0471	4.00
44	R62	R: FX CFLM 1.0K OHM 5% 1/4W	116.2101	0.00
44	R6,R11,R22,R23,R24,R25,R26	R: FX CFLM 1.0K OHM 5% 1/4W	116.2101	8.00
46	R47	R: FX CFLM 1.5K OHM 5% 1/4W	116.2151	0.00
46	R17 THRU R21,R35,R38,R43,	R: FX CFLM 1.5K OHM 5% 1/4W	116.2151	9.00
48	R27 THRU R31,R40	R: FX CFLM 330 OHM 5% 1/4W	116.1331	6.00
50	R33,R39,R42,R46	R: FX CFLM 6.8K OHM 5% 1/4W	116.2681	4.00
52	R34	R: FX CFLM 220 OHM 5% 1/4W	116.1221	1.00
54	R45,R48	R: FX CFLM 150 OHM 5% 1/4W	116.1151	2.00
56	R49,R51	R: FX CFLM 4.7 OHM 5% 1/4W	116.9471	2.00
60	R53,R54,R63	R: FX CFLM 470 OHM 5% 1/4W	116.1471	3.00
62	R59,R60,R61	R: FX CFLM 100 OHM 5% 1/4W	116.1101	3.00
64	R50	R: FX MFLM 2.21K 1% 1/10W T2	111.2211	1.00
66	R52	R: FX MFLM 681 OHM 1% 1/10W T2	110.6811	1.00
67	C1,C4,C5,C9 THRU C16	C: FX CER .001UF 10% X5F 500V	100.2105	11.00
69	C2,C8,C17, THRU C21	C: FX CER 220PF 10% X5F	100.1225	7.00
71	C3,C6,C7,C60	C: FX CER .05UF 20% YSP 25V	100.3501	4.00
71	C3,C6,C7,C60	C: FX CER .05UF 20% YSP 25V	100.3501	4.00
73	C22,C64	C: FX CER 68PF 5% N750 500V	100.0687	2.00

WAVETEK SD INC. DWG NO. 02 004 5165 REV A

PC ASSY: DM

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
75	C23,C24,C32,C35,C41,C45	C: FX CER 22PF 5% NPO 500V	100.0229	6.00
77	C25,C29,C30,C39,C52,C53,C40	C: FX CER .01UF +80 -20% 50V	100.3101	7.00
79	C26	C: FX CER 27PF 5% NPO 500V	100.0279	1.00
81	C28,C37,C38,C51	C: FX CER 5.6PF .25PF NPO 500V	100.9509	4.00
83	[illegible]	C: FX CER 47PF 5% NPO 500V	100.0479	1.00
85	C46	C: FX CER 15PF 5% NPO 500V	100.0159	1.00
87	C48	C: FX CER 3.3PF .5PF NPO 500V	100.9339	1.00
89	C49,C61,C63,C57,C59,C54	C: FX CER 10PF 5% NPO 500V	100.0109	6.00
91	C56	C: FX CER 2.2PF .5PF NPO 500V	100.9229	1.00
95	C34,C43	C: FX MLD COMP 0.68PF 5% (QC)	107.8681	2.00
97	C62	C: VAR CER 1.2-10PF 5% 500V	100.0100	1.00

SECTION 11
DIGIT MODULE A

11.1 INTRODUCTION

The digit module A (DMA) generates the 1 MHz digit. This module is very similar to the DM module which feeds it. As well as containing the 1 MHz steps, the DMA module output (140.000 to 149.999,999,9 MHz) also contains all the finer steps down to 0.1 Hz.

The digit module A is housed in a frame and U-cover enclosure and plugs into three ten-pin connectors with asymmetric spacing to assure proper orientation. It can be removed as a complete unit after releasing the three screws located at the bottom of the deck.

11.2 THEORY OF OPERATION

The DMA module uses fixed bus signal frequencies from the SGA and SGB modules to modify the signal from the DM module (between 14.000 and 14.999 MHz). In effect, the DMA module moves each digit above the decimal point one position to the left and inserts a new digit (the DMA dial setting as programmed from either the front panel or a remote connector) in the space provided. For example, if the DMA input signal is 14.321 MHz and the DMA dial setting is "6", the DMA output signal will be 146.321 MHz. The DMA output signal is used as an input to drive the mixer in the 875 AMP/Mixer module through a 50Ω pad.

The fixed bus frequencies used in the DMA module are 14, 16, 18, 20, 22, 112, and 113 MHz. They are crystal oscillator derived and coherent. For any DMA dial setting selected, the DMA module uses either 112 MHz (for all even digits) or 113 MHz (for all odd digits) and one of the five lower frequencies, 14 MHz for digits 0 and 1, 16 MHz for digits 2 and 3, 18 MHz for digits 4 and 5, and so on.

Refer to schematic 03-004-5152. The 14.000 to 14.999 MHz signal from the DM module (14.321 for this example) enters the DMA module at J3 pin 3 where it is fed to the base of Q10, an additive mixer. The digit 1 control line, (pin 5) selects either Q1 or Q2 to direct the appropriate frequency (112 or 113 MHz respectively) to the base of Q10. Since the digit used in this example is even (6), J3 pin 5 and U1 pin 5 are low, putting a high at U1 pin 6, a low at U2 pin 11 and the base of Q1. With Q1 selected, Q10 mixes the 112 MHz signal from the SGB module with the 14.321 MHz signal from the digit module. The sum of the two inputs (112 MHz plus 14.321 MHz) is 126.321 MHz. Two 126-128 MHz double-tuned filters (C32 to C45 and associated components) along with amplifier Q11 select the upper sideband and filter out unwanted frequencies.

The 126.321 MHz signal from the first mixer is amplified by Q15 before entering a second additive mixer (M1). One of the switch-transistors, Q3 through Q7 provides the second input to this mixer. Since the digit used in this example is 6, J3 pins 6 and 7 are high and U2 pin 8 selects the 20 MHz signal at J4 pin 26 by placing a low at the base of Q6. Q16 amplifies the 20 MHz output of Q6, applying it to mixer M1, where it is summed with the 126.321 MHz signal to produce 146.321 MHz. As with the previous mixer, two double-tuned filters (C46 to C59 and associated components) along with amplifier Q12 select the upper sideband while suppressing the lower sideband and other unwanted frequencies.

A third filter (C94 to C99 and associated components) removes unwanted signals and feeds frequencies between 140 and 150 MHz to the DMA module output at pin 50. Effectively, a "6" has been placed between the decimal point and "14" in the digit module "A" input frequency of 14.321 MHz, producing an output frequency of 146.321 MHz.

11.3 SPECIFICATIONS

The specifications of the DMA module are as follows:

Input Signals	14 to 14.999,999,9 MHz 14, 16, 18, 20, and 22 MHz 112 and 113 MHz
Digit Control	1, 2, 4, and 8 BCD (positive true) High = +3.0V minimum. Low = +0.5V maximum.
Output Signals	140 to 149.999,999,9 MHz
DC Supply	+5.4V at 85 mA. −12.4V at 40 mA.
Connectors	Three 10-pin edgecard.

11.4 MAINTENANCE

11.4.1 Preventive Maintenance

Preventive maintenance is not required for the digit module "A" assembly. Normal operation is indicated by the presence of correct outputs. Minor aging effects will not impair operation.

11.4.2 Alignment/Calibration

Field or customer alignment of this assembly is not advised. If realignment is required, return the assembly to the factory for service.

11.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If the digit module "A" has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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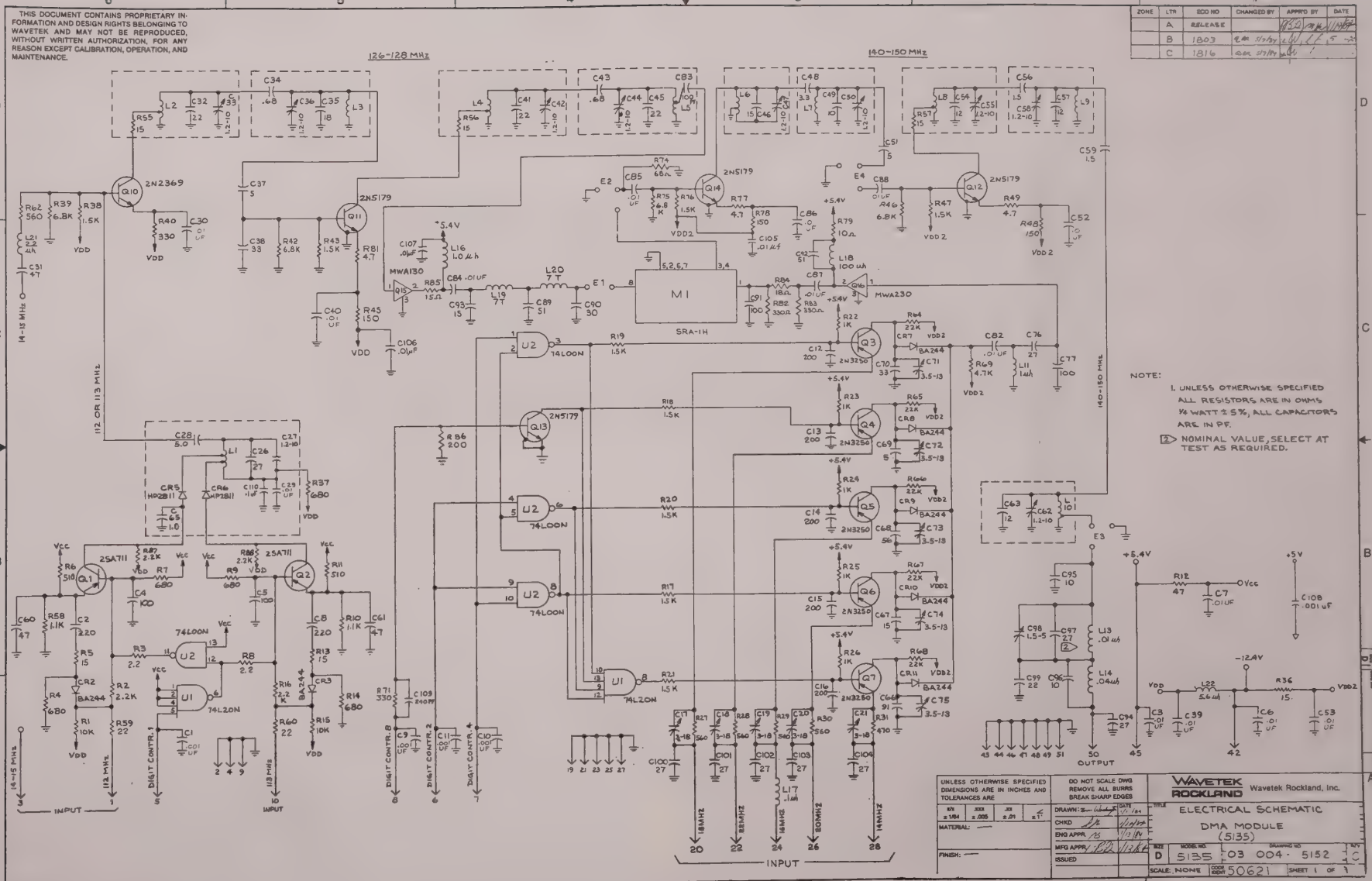
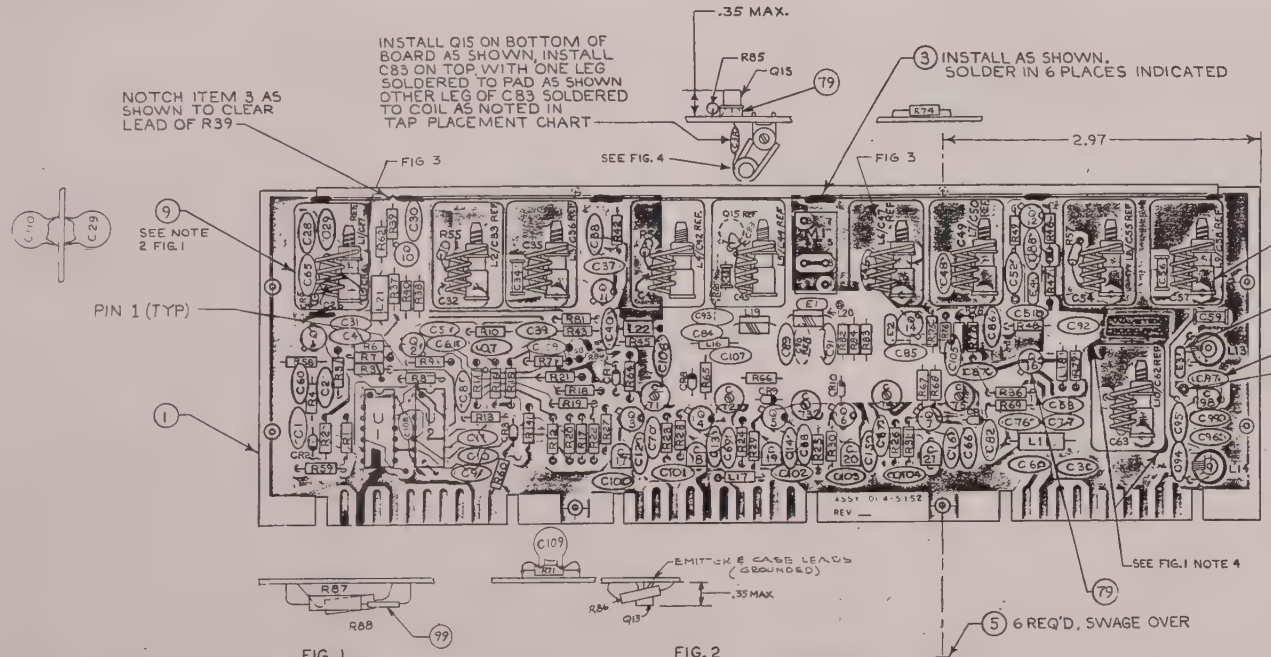
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	1803			
	C	1816			



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
.X ± .1 .XX ± .05 .XXX ± .025 ANG ± 1°	DRAWN: DATE	TITLE: ELECTRICAL SCHEMATIC DMA MODULE (5135)
MATERIAL:	CHKD	
FINISH:	ENG APPR.	
	MFG APPR.	SIZE D · MODEL NO. 5135 · DRAWING NO. 03 004 5152 · REV C
	ISSUED	SCALE: NONE · CODE IDENT 50621 · SHEET 1 OF 7

11-3

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	REL			
	B	303			
	C	1816			



TAP PLACEMENT CHART		
COIL	TURNS	TAP WITH
L1	2.0	CR6 CATHOD
L1	2.25	CR5 CATHOD
L2	1.5	R55
L4	1.5	R56
L5	.25	C83
L6	1.75	BUSS TO GND
L8	3.5	R57
L10	.75	BUSS TO PAD

FIG. 1
C27 REF.

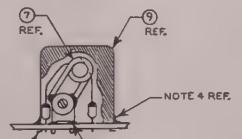


FIG. 2

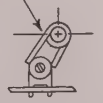
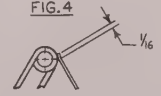


FIG. 3

FIG. 4



NOTES:
1. TUNED CIRCUIT ASSY. ITEM 7 TYP 10 PLACES L1-L10
2. SHIELD ASSY. ITEM 9 INSTALLED IN TEST, TYP 10 PLACES
3. HOLDING SHIELD FIRMLY TO BOARD, BEND PINS OVER AND SOLDER
4. SOLDER TWO OPPOSITE CORNERS OF COVERS AS SHOWN 20 PLACES
5. SOLDER CAPACITOR TO GROUND PLANE FOR C33,36,42,44,50,55,58,62 FOR SOLDERING C27 & C47 SEE FIG. 3

6 NOMINAL VALUE (27PF) ITEM 21 INSTALLED. SELECT AT TEST AS REQUIRED.

COUNTING TURNS FOR TAP PLACEMENT: BEGIN COUNTING AT "R" THE 9 O'CLOCK POSITION ON THE COIL NEAR THE ADJUST END OF THE TRIMMER CAPACITOR AS SHOWN ABOVE IN REF. TO TAP PLACEMENT CHART AND FIG. 4

C27 AND C47 SHOULD BE RAISED ABOVE BOARD AS SHOWN

TYP SOLDERING OF TAP TO COIL LEAVING NO SLACK IN TAP WIRE

SHEETS 2,3,& 4 ARE "A" SIZE L/M

DR		DATE 11/1/64	WAVETEK ROCKLAND Wavetek Rockland, Inc.
CHKD			P.C. ASSEMBLY DMA MODULE (5135)
ENG.		11/14/67	
MFG.		11/16/67	
ISSUED			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE			SIZE D · MODEL NO 5135 · DRAWING NO 02-004-5152 · REV C
MAT			SCALE 2:1 · CODE IDENT 50621 · SHEET 1 OF 4
FIN			

WAVETEK SD INC. DWG NO. 02 004 5152 REV C

PC ASSY: DMA

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: "DMA" MODULE 5120	320.5150	1.00
3	-	GROUND STRIP ASSY "DMA" MODULE	011.2200	1.00
5	-	SPR: THD .156D 2-56 X 3/16 SWG	389.2021	6.00
7	(L10,C62)REF	TUNED CKT ASSY: 5600	012.7401	0.00
7	(L7,C58)(L8,C55)(L9,C58)	TUNED CKT ASSY: 5600	012.7401	0.00
7	(L1,C27)(L2,C33)(L3,C36)	TUNED CKT ASSY: 5600	012.7401	10.00
7	(L4,C42)(L5,C44)(L6,C47)	TUNED CKT ASSY: 5600	012.7401	0.00
9	FOR L1-L10	SHIELD ASSY: 5600	012.6201	10.00
10	L21	L: FXD 2.2 UHY +/-10%	150.9222	1.00
11	6"	WIRE: BUSS HD DWN TND #20 AWG	378.0500	1.00
12	L18	L: FXD 100 UHY +/-10% MINI.	150.1101	1.00
13	L17	L: FXD .10 UHY +/-10% MINI.	150.8101	1.00
14	C89,C92	C: FX MICA DP 51PF +-5% 500V	101.0510	2.00
15	C90	C: FX MICA DP 30PF +-5% 500V	101.0300	1.00
16	C1,C9-C11,C108	C: FX CER .001UF 10% X5F 500V	100.2105	5.00
17	C2.C8	C: FX CER 220PF 10% X5F	100.1225	2.00
18	C52,C53,C82,C84-88,C105-107	C: FX CER .01UF +80 -20% 100V	100.3104	0.00
18	C3,C6,C7,C29,C38,C39,C40,	C: FX CER .01UF +80 -20% 100V	100.3104	18.00
20	C31,C60,C61	C: FX CER 47PF 5% NPO 500V	100.0479	3.00
21	C26,C76,C94,C100-C104,C97	C: FX CER 27PF 5% NPO 500V	100.0279	9.00
22	C28,C37,C51,C69	C: FX CER 5.0PF .25PF NPO 500V	100.9509	4.00
23	C32,C41,C45,C99	C: FX CER 22PF 5% NPO 500V	100.0229	4.00
24	C34,C43	C: FX CRM TUB .68PF .25PF NPO	106.8689	2.00
25	C38,C78	C: FX CER 33PF 5% NPO 500V	100.0339	2.00
26	C46,C67,C93	C: FX CER 15PF 5% NPO 500V	100.0159	3.00
27	C48	C: FX CER 3.3PF .5PF NPO 500V	100.9339	1.00
28	C49,C95,C96	C: FX CER 10PF 5% NPO 500V	100.0109	3.00
29	C54,C57,C63	C: FX CER 12PF 5% NPO 500V	100.0129	3.00
30	C56,C59	C: FX CRM TUB 1.5PF .25PF NPO	106.9159	2.00
31	C71-C75	C: VAR CER 3.5-13PF 5% 500V	100.0130	5.00
32	C65	C: FX CRM TUB 1.0PF .25PF NPO	106.9109	1.00
33	C17-C21	C: VAR CER 3.5-18PF 250V	100.0100	5.00
34	C66	C: FX CER 91PF 5% N750 500V	100.0917	1.00
35	C98	C: VAR CER 1.5-5PF 250V	100.0050	1.00
36	C91,C77,C83,C4,C5	C: FX CER 100PF 10% X5F 500V	100.1105	5.00
37	C68	C: FX CER 56PF 5% NPO 500V	100.0569	1.00
38	C35	C: FX CER 18PF 5% NPO 500V	100.0189	1.00
40	R10,R58	R: FX CFLM 1.1K OHM 5% 1/4W	116.2111	2.00
41	R6,R11	R: FX CFLM 510 OHM 5% 1/4W	116.1511	2.00
42	R3,R8	R: FX CFLM 2.2 OHM 5% 1/4W	116.9221	2.00
43	R69	R: FX CFLM 4.7K OHM 5% 1/4W	116.2471	1.00
44	R1,R15	R: FX CFLM 10K OHM 5% 1/4W	116.3101	2.00

WAVETEK SD INC. DWG NO. 02 004 5152 REV C

PC ASSY: DMA

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
45	R2,R16,R87,R88	R: FX CFLM 2.2K OHM 5% 1/4W	116.2221	4.00
46	R5,R13,R36,R55-R57,R85	R: FX CFLM 15 OHM 5% 1/4W	116.0151	7.00
47	R4,R9,R14,R37,R7	R: FX CFLM 680 OHM 5% 1/4W	116.1681	5.00
48	R12	R: FX CFLM 47 OHM 5% 1/4W	116.0471	1.00
49	R22-R26	R: FX CFLM 1.0K OHM 5% 1/4W	116.2101	5.00
50	R17-R20,R76,R38,R43,R47,R21	R: FX CFLM 1.5K OHM 5% 1/4W	116.2151	9.00
51	R31	R: FX CFLM 470 OHM 5% 1/4W	116.1471	1.00
52	R75,R39,R42,R46	R: FX CFLM 6.8K OHM 5% 1/4W	116.2681	4.00
53	R84	R: FX CFLM 18 OHM 5% 1/4W	116.0181	1.00
54	R40,R71,R82,R83	R: FX CFLM 330 OHM 5% 1/4W	116.1331	4.00
55	R45,R46,R78	R: FX CFLM 150 OHM 5% 1/4W	116.1151	3.00
56	R49,R77,R81	R: FX CFLM 4.7 OHM 5% 1/4W	116.9471	3.00
57	R59,R60	R: FX CFLM 22 OHM 5% 1/4W	116.0221	2.00
58	R86	R: FX CFLM 200 OHM 5% 1/4W	116.1201	1.00
59	R64-R68	R: FX CFLM 22K OHM 5% 1/4W	116.3221	5.00
60	R79	R: FX CFLM 10 OHM 5% 1/4W	116.0101	1.00
61	R27-R30,R62	R: FX CFLM 560 OHM 5% 1/4W	116.1561	5.00
62	R74	R: FX CFLM 68 OHM 5% 1/4W	116.0681	1.00
64	L11,L16	L: FXD 1.0 UHY +/-10%	150.9102	2.00
65	L19,L20	L: TOROIDAL 7 TURN	012.1058	2.00
66	L22	L: FXD 5.6 UHY +/-10%	150.9562	1.00
67	Q1,Q2	Q: SIL PNP (2SA711)	137.0711	2.00
68	Q3-Q7	Q: SIL PNP (2N3250)	136.3250	5.00
69	Q10	Q: SIL NPN (2N2369)	134.2369	1.00
70	Q11-Q14	Q: SIL NPN (2N5179)	134.5179	4.00
72	FOR Q15,Q16	SPACER: TXSTR LEAD, NYL, LOW	376.2100	2.00
73	Q16(MWA230)	U: WIDE BAND HYB AMP DC-600MHZ	120.7230	1.00
74	Q15(MWA130)	U: WIDE BAND HYB AMP DC-400MHZ	120.7130	1.00
75	L13	L: TOROIDAL, 5150 MOD. .01UHY	012.1054	1.00
76	L14	L: TOROIDAL, 5150 MOD. .04UHY	012.1055	1.00
77	CR5,CR6	CR: SCHOTTKY BARRIER	133.2811	2.00
78	CR2-CR3,CR7-CR11	CR: SWITCHING (BA482 OR BA244)	133.0244	7.00
80	M1	U: DBL BAL MIXER (SRA-1H) GRD	129.5000	1.00
82	U1	U: DUAL 4 IN NAND GATE	121.7420	1.00
83	U2	U: QUAD 2 IN NAND GATE	121.7400	1.00
85	E1-E4	PLUG: SHORTING (LOW PROF)	352.0202	4.00
87	TEST POINT GROUNDS	SOCKET: JMPR (USE W/352.0202)	353.0104	3.00
89	E1-E4	SOCKET: JUMPER	353.0103	8.00
91	C12-C16	C: FX MICA DP 200PF +-5% 500V	101.1200	5.00
95	C109	C: FX MICA DP 240PF +-5% 500V	101.1240	1.00
97	C110	C: FX MONO 0.1UF Z5U 50V	100.4102	1.00
99	FOR R88	SLVNG: PLASTIC FBRGLS #22AWG	378.5221	1.00

SECTION 12
PHASE LOCKED LOOP CIRCUITS

12.1 INTRODUCTION

The Phase Locked Loop (PLL) and Voltage Controlled Oscillator (VCO) circuits provide the synthesizer with 10 and 100 MHz resolution steps. Inputs to the PLL/VCO module are the 10 MHz reference from the SGA module and the digital frequency control from the front panel. The voltage controlled oscillator board output drives the distribution amplifier, which in turn drives the picket fence mixer and the output mixer. The distribution amplifier also provides an amplified sample of the VCO output as feedback to the phase locked loop for correction voltage generation.

12.2 THEORY OF OPERATION

12.2.1 Phase Locked Loop

Refer to block diagram figure 12-1. (The phase locked loop schematic is proprietary to Wavetek and therefore not included.) The voltage controlled oscillator output signal, which has a frequency of between 735 and 1225 MHz depending upon the programmed frequency of the synthesizer, enters the PLL circuit via the distribution amplifier. Divider 1 in the phase lock loop circuit divides this signal by 4 before entering the ÷ 294 to ÷ 490 (divider 2) circuit. Divider 2 is controlled by the front panel and always produces an output frequency of 625 kHz.

Suppose the VCO output frequency is 800 MHz. Divider 1 produces an output of 200 MHz which is applied to divider 2. The front panel control programs divider 2 to divide this 200 MHz signal by 320, producing a 625 kHz signal as one input to the phase detector. The 10 MHz reference from the SGA module is divided by 16, producing a frequency of 625 kHz at the second phase detector input. Any difference in frequency or phase of the two phase detector inputs produces a rapid voltage change at the low pass filter input. This filter smooths out the rapid changes and causes the VCO to modify its output frequency (see paragraph 12.2.2). In this way, the phase lock loop circuit holds the VCO output frequency at 800 MHz.

12.2.2 Voltage Controlled Oscillator

Refer to block diagram figure 12-1. (The voltage controlled oscillator schematic is proprietary to Wavetek and therefore not included.) The VCO produces an output frequency of between 735 and 1225 MHz, depending upon the programmed frequency of the synthesizer. The VCO contains four nearly identical oscillators driven by a single amplifier. The oscillator used for any programmed frequency is determined for the Model 5156A by the logic levels of U52 pins 2 and 5 on the remote front panel board 002.5422, and for the Model 5155A by the logic levels of U47 pins 2 and 5 on the front panel board 002.5423. The amplifier driving these oscillators is controlled by the PLL low pass filter output. Together, these four oscillators produce the 735 to 1225 MHz signal that, through an RF amplifier, drives the distribution amplifier.

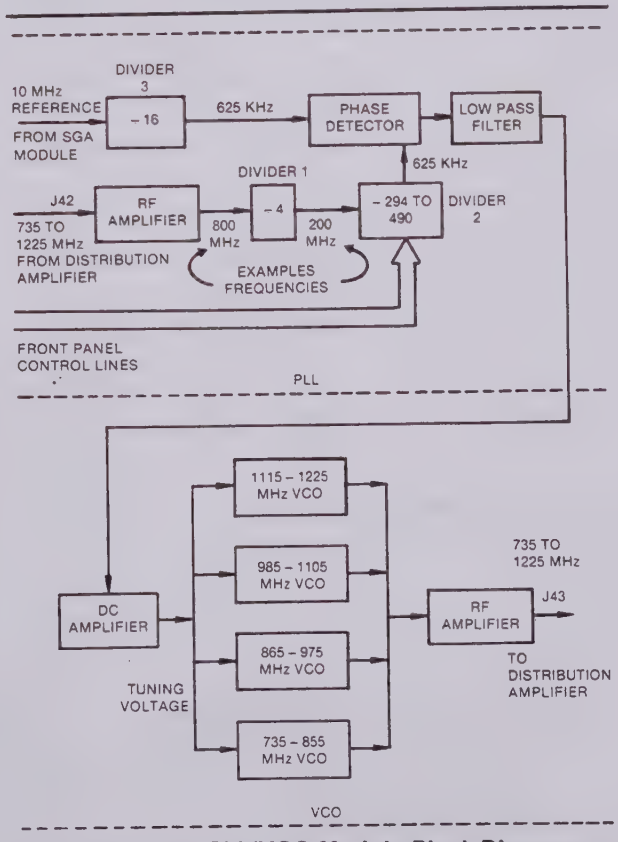


Figure 12-1. PLL/VCO Module Block Diagram

12.2.3 Distribution Amplifier

The distribution amplifier splits the 735 to 1225 MHz VCO output frequency signal for use by several frequency generator circuits as well as the PLL circuit. Refer to schematic 03-004-5484. The 735 to 1225 MHz signal from the VCO enters the distribution amplifier through J73, is amplified by AR1, then split in three directions. One portion is amplified by AR4, then attenuated 8 dB by R11, R12 and R13 before exiting the circuit at J75. The second portion is amplified by AR2, attenuated by 10 dB pad R5, R6 and R7, then amplified by AR3. This signal is output at J76. The third portion of the input signal is amplified by AR5, then attenuated 3 dB by R16, R17 and R18, and exits at J74. These signals drive the PF mixer and output mixers, and the PLL circuit.

12.3 SPECIFICATIONS

12.3.1 Phase Locked Loop

Control Panel Inputs	DRU 2, 4, and 8. DRT 1, 2, 4, and 8. DRH 1 and 2.
Input Signals	10 MHz Reference. 735 to 1225 MHz sample frequency.
Output Signal	DC error voltage to VCO.
DC Supply	+ 5.4V at 300 mA. – 12.4V at 10 mA. + 28V at 60 mA.
Connectors	Two 10-pin edgecard. One SMA female.

12.3.2 Voltage Controlled Oscillator

Input Signal	DC error voltage from PLL.
Output Signal	735 to 1225 MHz RF.
DC Supply	+ 5.4V at 55 mA. + 28V at 150 mA.
Connector	One SMA female.

12.3.3 Distribution Amplifier

Input Signal	735 to 1225 MHz.
Output Signals	
PF Mixer Input	735 to 1225 MHz.
Output Mixer Input	735 to 1225 MHz.
PLL Feedback Input	735 to 1225 MHz.
DC Supply	+ 6.0V at 140 mA.
Connectors	Four SMA female.

12.4 MAINTENANCE

12.4.1 Preventive Maintenance

Preventive maintenance is not required for the phase locked loop (containing the voltage controlled oscillator) or distribution amplifier modules. Normal operation is indicated by the presence of correct outputs.

12.4.2 Alignment/Calibration

Field or customer alignment of the phase locked loop, voltage controlled oscillator or distribution amplifier modules is not advised. No alignment of the distribution amplifier is required. If realignment of the phase locked loop or voltage controlled oscillator is required, return the assembly to the factory for service.

12.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If the distribution amplifier has been isolated as the source of the problem, faulty active amplifiers may be replaced. Careful use of printed circuit repair techniques as applicable to double-sided boards with plated through holes is strongly advised. No realignment is necessary after replacing faulty components.

If the phase locked loop or voltage controlled oscillator have been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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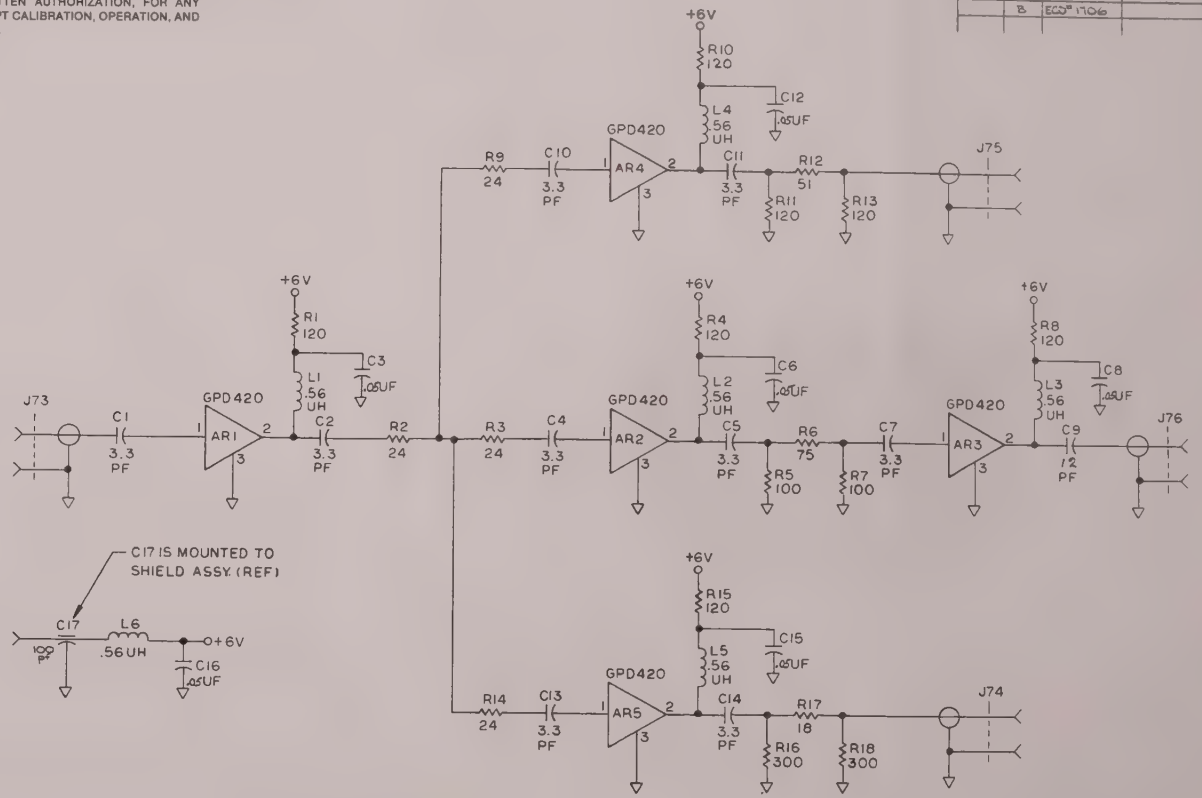
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE			1/25/84
	B	ECO# 1706			7/5/84



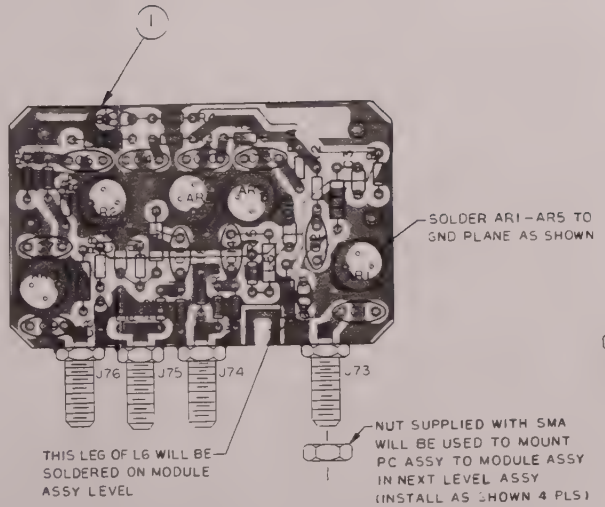
NOTE

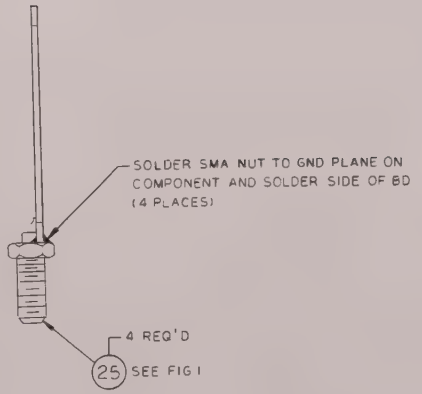
1. ALL RESISTORS ARE IN OHMS AND ARE 1/8 W, 5%

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
x/x ±1/64 .xxx ±.005 .xx ±.01 ±1°	DRAWN: M. McMinn DATE 1/20/84	TITLE: ELECTRICAL SCHEMATIC DISTRIBUTION AMP
MATERIAL:	CHKD	
FINISH:	ENG APPR 1/25/84	
	MFG APPR. 1/26/84	SIZE C MODEL NO. 5150 DRAWING NO. 03-004-5484 REV B
	ISSUED	SCALE: — CODE IDENT 50621 SHEET 1 OF 1

R.S. KNAPP

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			1/29/84


1
J76
J75
J74
J73
SOLDER AR1-AR5 TO GND PLANE AS SHOWN
THIS LEG OF L6 WILL BE SOLDERED ON MODULE ASSY LEVEL
NUT SUPPLIED WITH SMA WILL BE USED TO MOUNT PC ASSY TO MODULE ASSY IN NEXT LEVEL ASSY (INSTALL AS SHOWN 4 PLS)



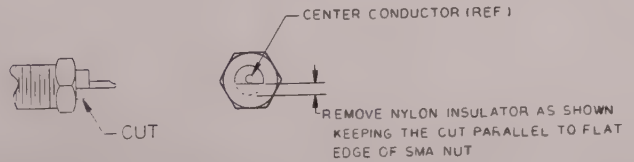


FIG 1

SHEET 2 IS "A" SIZE L/M

DR M. McMINN	DATE 1/19/84	WAVETEK ROCKLAND Wavetek Rockland, Inc.
CHKD		
ENG		PC ASSY DISTRIBUTION AMP
MFG	1/25/84	
ISSUED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/8 ± 1/64	xxx ± .005	xx ± .01	∠ ± 1°

MAT —

FIN —

SIZE	MODEL NO	DRAWING NO	REV
C	5510	02-004-5484	E
SCALE 2:1	CODE IDENT 50621	SHEET 1 OF 2	

WAVETEK SD INC. DWG NO. 02 004 5484 REV B

PC ASSY: DISTRIBUTION AMP

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: DISTRIBUTION AMP	320.5484	1.00
3	AR1-AR5	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7420	5.00
5	R1,R4,R8,R10,R11,R13,R15	R: FX CFLM 120 OHM 5% 1/8W	116.1120	7.00
7	R2,R3,R9,R14	R: FX CFLM 24 OHM 5% 1/8W	116.0240	4.00
9	R5,R7	R: FX CFLM 100 OHM 5% 1/8W	116.1100	2.00
11	R6	R: FX CFLM 75 OHM 5% 1/8W	116.0750	1.00
13	R12	R: FX CFLM 51 OHM 5% 1/8W	116.0510	1.00
15	R16,R18	R: FX CFLM 300 OHM 5% 1/8W	116.1300	2.00
17	R17	R: FX CFLM 18 OHM 5% 1/8W	116.0180	1.00
19	C14	C: FX CER 3.3PF .5PF NPO 500V	100.9338	0.00
19	C1,C2,C4,C5,C7,C10,C11,C13,	C: FX CER 3.3PF .5PF NPO 500V	100.9338	9.00
21	C3,C6,C8,C12,C15,C16	C: FX CER .05UF +20-80 Y5F 12V	100.3502	6.00
23	L1-L6	L: FXD .56 UHY +/-10% MINI.	150.8561	6.00
25	J73-J76	CONN: SMA BULK RECPT .5"	351.0023	4.00
26	C9	C: FX CER 12PF 5% NPO 500V	100.0129	1.00

SECTION 13
PICKET FENCE MIXER CIRCUITS

13.1 INTRODUCTION

The picket fence mixer consists of the 10 MHz harmonic generator and the picket fence mixer (PF mixer). The 10 MHz harmonic generator accepts the 10 MHz signal from the SGA module, creating a picket fence signal of 10 to 350 MHz. This is one of two inputs to the PF mixer, the second being one of the signals (at the VCO output frequency) from the distribution amplifier. The PF mixer output is used to drive the comb amplifier/filter.

13.2 THEORY OF OPERATION

13.2.1 10 MHz Harmonic Generator

The 10 MHz harmonic generator creates a picket fence signal of 10 to 350 MHz from the 10 MHz SGA module output. This signal is used as one of two inputs to the PF mixer. Refer to schematic 03-004-5483. The 10 MHz harmonic generator receives the 10 MHz signal from the SGA module. This signal at J27 is the input to a pad consisting of R1, R2 and R3. The signal then passes through a 10 MHz low pass filter (C1, C2 and L1) which further attenuates the signal by 1 dB before amplifier AR1 increases the signal strength by 14 dB. R4, R5 and R6 attenuates this signal before entering the SRD comb circuit, which creates the comb (or picket fence) frequencies. The signal is then attenuated by R8, R9 and R10 before entering the bandpass filter consisting of C11, C12 and L6. This output signal at J28 is one input to the PF mixer.

13.2.2 Picket Fence Mixer

The picket fence mixer (PF mixer) combines the picket fence signal from the harmonic generator with one of the VCO frequency outputs from the distribution amplifier to drive the comb amplifier/filter. Refer to schematic 03-004-5485. The PF mixer receives the 10 to 350 MHz picket fence from the harmonic generator at J34 and a 735 to 1225 MHz output from the distribution amplifier at J33. The signal at J34 is input to a pad consisting of R10, R12 and R13 before entering mixer M1. The distribution amplifier signal is attenuated by a pad consisting of R7, R8 and R9, then passes through three amplifiers (AR1, AR2 and AR3) with gains of 11, 10 and 9 respectively. The signal is attenuated before reaching mixer M1 at pin 8. The mixer output has a number of possible frequency combinations, but always contains an 875 MHz signal. A pad (R13, R14 and R15) feeds the output signal via J35 to the comb amplifier/filter.

13.3 SPECIFICATIONS

13.3.1 10 MHz Harmonic Generator

Input Signal	10.000000 MHz Reference.
Output Signal	10 to 350 MHz harmonics.
DC Supply	+6.0V at 75 mA.
Connectors	Two SMA female.

13.3.2 Picket Fence Mixer

Input Signals	10 to 350 MHz harmonics. 735 to 1225 MHz.
Output Signal	875 MHz.
DC Supply	+6.0V at 105 mA.
Connectors	Three SMA female

13.4 MAINTENANCE

13.4.1 Preventive Maintenance

Preventive maintenance is not required for the 10 MHz harmonic generator or the picket fence mixer module. Normal operation is indicated by the presence of correct outputs.

13.4.2 Alignment/Calibration

No alignment or calibration is necessary after replacement of individual parts.

13.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before attempting to replace an assembly.

If either the 10 MHz harmonic generator or picket fence mixer module have been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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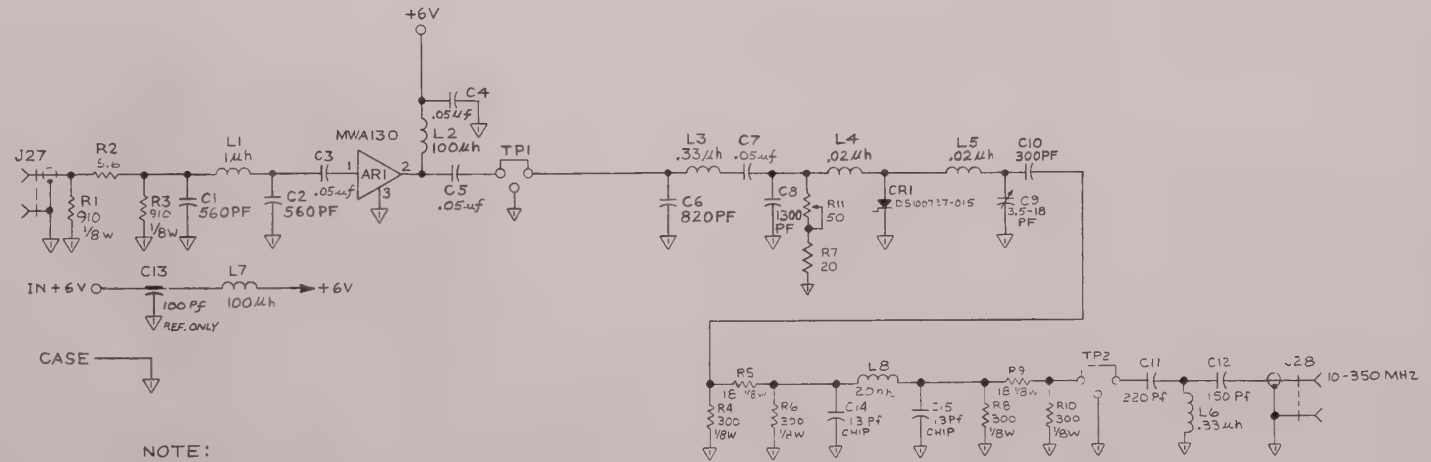
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	PROTO			11/1/83
	B	1706	JP		3/14/84
	C	2003	M McMINN		7/23/85
	D	2081	N.R 1/30/86		1/31/86
	E	2100	M.McMINN		3/7/86
	F	2140	M.McMINN		7/14/86



NOTE:
1. UNLESS OTHERWISE SPECIFIED.
   a) ALL RESISTORS ARE IN OHMS ±5%, 1/4W.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND	Wavetek Rockland, Inc.
x/x ±1/64 .xxx ±.005 .xx ±.01 ∠ ±1°	DRAWN N. Peters DATE 8/4/83	TITLE	ELECTRICAL SCHEMATIC 10MHz HARMONIC GENERATOR
MATERIAL: —	CHKD JR 11/1/83		
FINISH: —	ENG APPR. RLS 11/1/83		
	MFG APPR. RLS 11.1.83	SIZE C	MODEL NO 5150
	ISSUED	DRAWING NO	03-004-5483
		REV	F
		SCALE: —	CODE IDENT 23332
		SHEET 1 OF 1	

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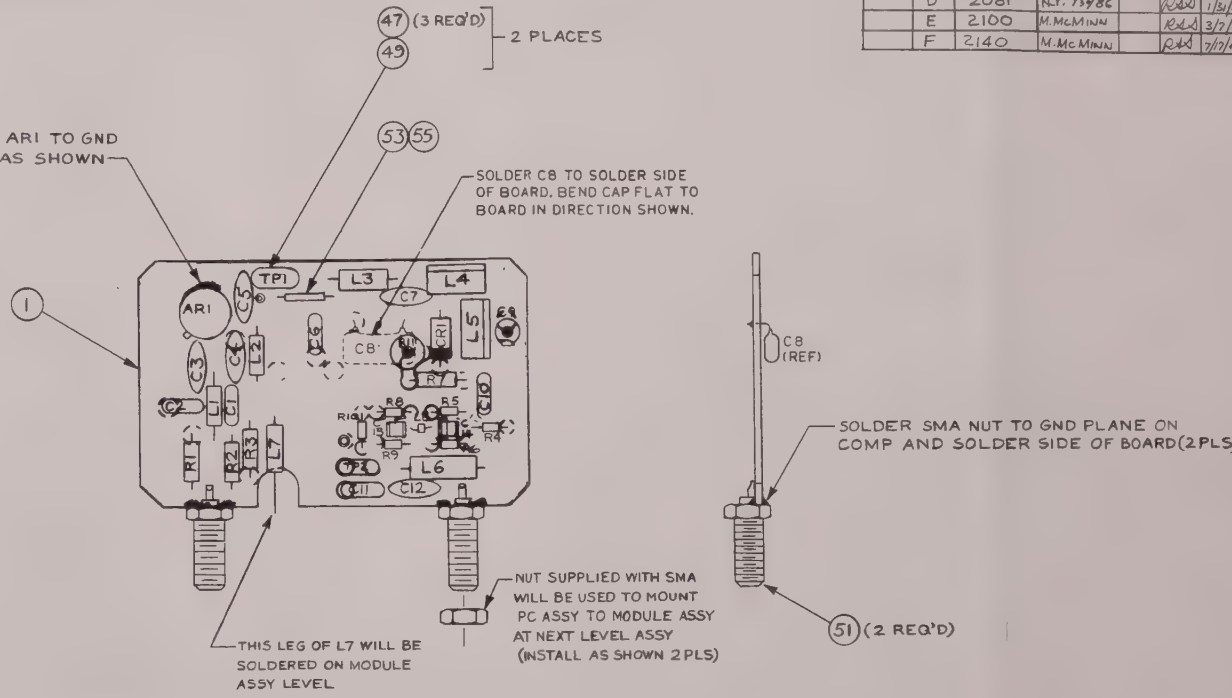
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			11/1/83
	B	1706	JP		1/5/84
	C	2003	M.McMINN		5/23/85
	D	2081	N.P. 9/30/86		1/5/86
	E	2100	M.McMINN		3/7/86
	F	2140	M.McMINN		7/17/86



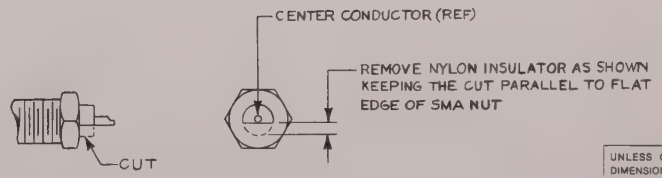


FIG 1

SHEET 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: X/X ±1/64, .XXX ±.005, .XX ±.01, ∠ ±1°

MATERIAL:

FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN	R. Peters	10/19/83
CHKD		11/1/83
ENG APPR		11/1/83
MFG APPR		11/1/83
ISSUED		

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: P.C. ASSY 10MHz HARMONIC GENERATOR

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5483	F

SCALE: 2:1 | CODE IDENT: 50621 | SHEET 1 OF 2

R.S. KNAPP

WAVETEK SD INC. DWG NO. 02-004-5483 REV F

PC ASSY: 10 MHZ HARMONIC GEN.

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: 10MHZ HARMONIC GEN.	320.5483	1.00
4	R1,R3,	R: FX CFLM 910 OHM 5% 1/8W	116.1910	2.00
5	R2,	R: FX CFLM 5.6 OHM 5% 1/4W	116.9561	1.00
7	R9,R5	R: FX CFLM 18 OHM 5% 1/8W	116.0180	2.00
9	R8,R10,R4,R6,	R: FX CFLM 300 OHM 5% 1/8W	116.1300	4.00
13	R7	R: FX CFLM 20 OHM 5% 1/4W	116.0201	1.00
14	R11	R: VAR CMT 50 OHM 1/4" RND	118.0501	1.00
15	C11,	C: FX CER 220PF 10% X5F	100.1225	1.00
17	C12	C: FX MICA DP 150PF +-5% 500V	101.1150	1.00
19	C10	C: FX MICA DP 300PF +-5% 500V	101.1300	1.00
21	C1,C2	C: FX MICA DP 560PF +-5% 500V	101.1560	2.00
23	C6	C: FX MICA DP 820PF +-5% 300V	101.1820	1.00
25	C8	C: FX MICA DP 1300PF +-1% 500V	101.2131	1.00
29	C3,C4,C5,C7,	C: FX CER .05UF +20-80 Y5F 12V	100.3502	4.00
31	C9	C: VAR CER 3.5-18PF 250V	108.0180	1.00
33	C14,C15,	C: FX CER CHIP 13PF	107.0132	2.00
35	L4,L5	L: TOROIDAL, 5150 MOD. .01UHY	012.1054	2.00
37	L3,L6	L: FXD .33 UHY +/-20%	150.8332	2.00
39	L1	L: FXD 1.0 UHY +/-10%	150.9102	1.00
41	L2,	L: FXD 100 UHY +/-10% MINI.	150.1101	1.00
43	AR1	U: WIDE BAND HYB AMP DC-400MHZ	120.7130	1.00
45	CR1	CR: STEP RECOVERY	133.3202	1.00
47	-	SOCKET: JMPR (USE W/352.0202)	353.0103	6.00
49	-	PLUG: SHORTING (LOW PROF)	352.0202	2.00
51	J27,J28	CONN: SMA BULK RECPT .5"	351.0023	2.00
53	6"	WIRE: BUSS TINNED #22GA	378.0601	1.00
55	6"	SLVNG: TEFLON #22AWG	378.5222	1.00
57	L7	L: FXD 100 UHY +/-10%	150.1100	1.00
59	L8	L:TOROID 8T T7/36AWG	012.1065	1.00

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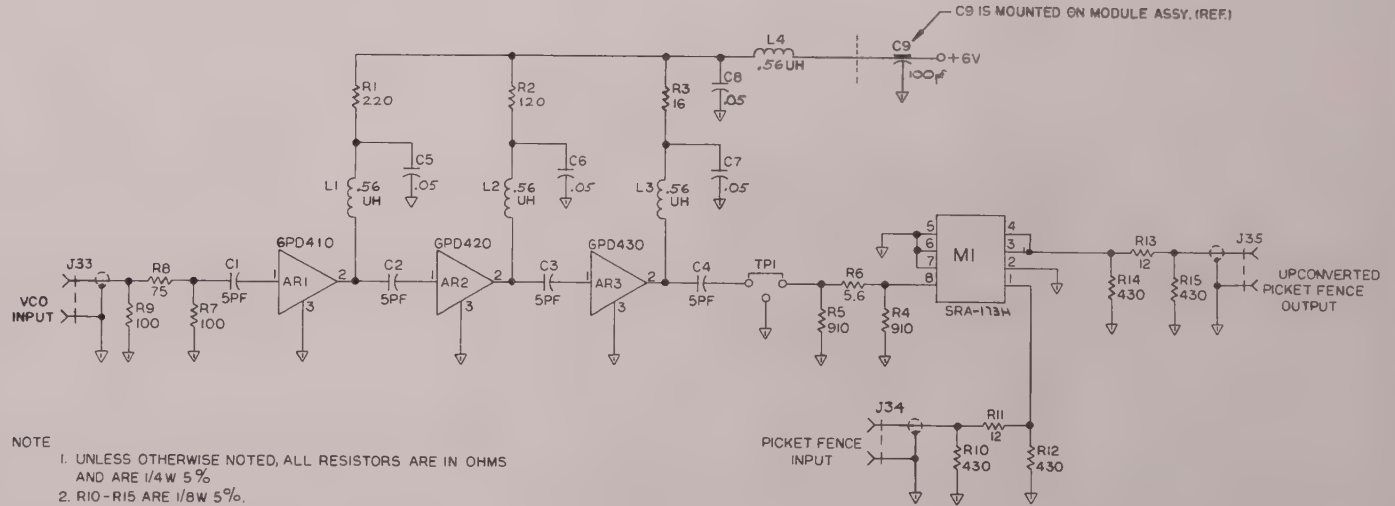
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE			11/1/83
	B	ECO# 1706			7/5/84
	C	ECO 1916	S.R. 11/15/84		9/1/87



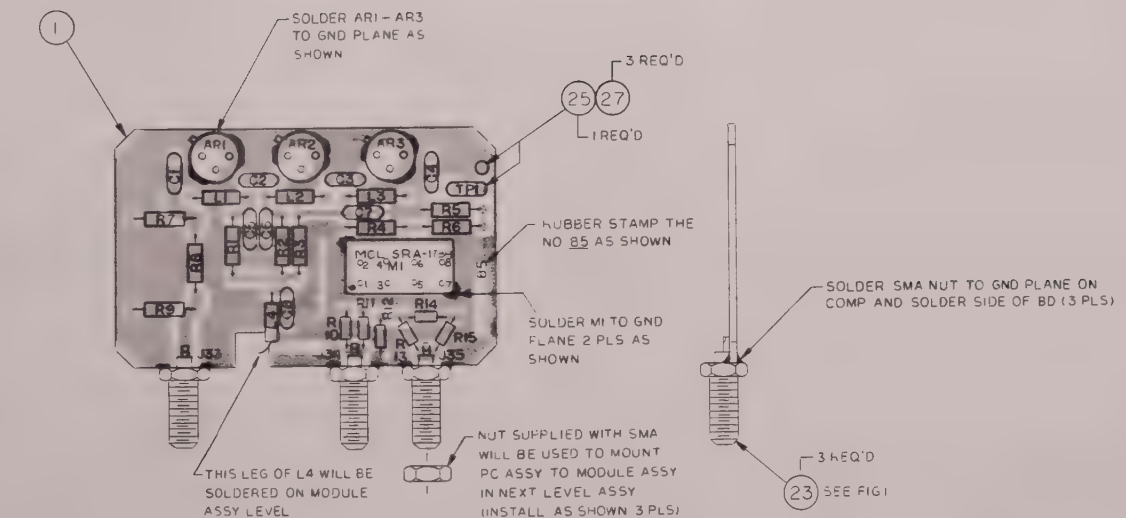
NOTE

1. UNLESS OTHERWISE NOTED, ALL RESISTORS ARE IN OHMS AND ARE 1/4W 5%
2. R10-R15 ARE 1/8W 5%.
3. UNLESS OTHERWISE NOTED, ALL CAPS ARE IN UF.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
x/x ±1/64 .xxx ±.005 .xx ±.01 ∠ ±1°	DRAWN M McMinn DATE 5-2-83	TITLE: ELECTRICAL SCHEMATIC PICKET FENCE-VCO MIXER
MATERIAL: ——	CHKD 11/1/83	
FINISH: ——	ENG APPR. 11/1/83	
	MFG APPR. 11/1/83	SIZE C · MODEL NO 5150 · DRAWING NO 03-004-5485 · REV C
	ISSUED	SCALE: —— · CODE IDENT 50621 · SHEET 1 OF 1

R.S. KNAPP

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	1706			
	C	3216			
	D	3331			


1
SOLDER AR1 – AR3 TO GND PLANE AS SHOWN
3 REQ'D
25
27
1 REQ'D
TP1
RUBBER STAMP THE NO 85 AS SHOWN
SOLDER M1 TO GND PLANE 2 PLS AS SHOWN
THIS LEG OF L4 WILL BE SOLDERED ON MODULE ASSY LEVEL
NUT SUPPLIED WITH SMA WILL BE USED TO MOUNT PC ASSY TO MODULE ASSY IN NEXT LEVEL ASSY (INSTALL AS SHOWN 3 PLS)
SOLDER SMA NUT TO GND PLANE ON COMP AND SOLDER SIDE OF BD (3 PLS)
3 REQ'D
23
SEE FIG 1

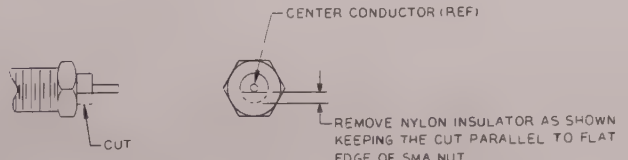


FIG 1

SHEET 2 IS "A" SIZE L/M

DR M. McMinn	DATE 3/9/83
CHKD	
ENG	
MFG	
ISSUED	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

.XX ± .01	.XXX ± .005	FRACTIONS ± 1/64	ANGLES ± 1°

MAT

FIN

WAVETEK ROCKLAND Wavetek Rockland, Inc.

PC ASSY
PICKET FENCE/VCO MIXER

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5485	C

SCALE 2:1 | CODE IDENT 50621 | SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5485 REV D

PC ASSY: VCO-PF MIXER

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: VCO-PF/.1-500 OUT MIXER	320.5485	1.00
3	AR1	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7410	1.00
4	AR2	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7420	1.00
5	AR3	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7430	1.00
6	M1	U: DBL BAL MIXER (SRA173H)	129.5006	1.00
8	R1	R: FX CFLM 220 OHM 5% 1/4W	116.1221	1.00
9	R2	R: FX CFLM 120 OHM 5% 1/4W	116.1121	1.00
10	R3	R: FX CFLM 16 0HM 5% 1/4W	116.0161	1.00
11	R4,R5	R: FX CFLM 910 OHM 5% 1/4W	116.1911	2.00
12	R6	R: FX CFLM 5.6 OHM 5% 1/4W	116.9561	1.00
13	R7,R9	R: FX CFLM 100 OHM 5% 1/4W	116.1101	2.00
14	R8	R: FX CFLM 75 OHM 5% 1/4W	116.0751	1.00
15	R10,R12,R14,R15	R: FX CFLM 430 OHM 5% 1/8W	116.1430	4.00
16	R11,R13	R: FX CFLM 12 OHM 5% 1/8W	116.0120	2.00
18	C1,C2,C3,C4	C: FX CER 5.0PF .25PF NPO 500V	100.9509	4.00
19	C5,C6,C7,C8	C: FX CER .05UF +20-80 Y5F 12V	100.3502	4.00
21	L1,L2,L3,L4	L: FXD .56 UHY +/-10% MINI.	150.8561	4.00
23	J33,J34,J35	CONN: SMA BULK RECPT .5"	351.0023	3.00
25	TP1	PLUG: SHORTING (LOW PROF)	352.0202	1.00
27	XTP1	SOCKET: JUMPER	353.0103	3.00

SECTION 14
COMB AMPLIFIER/FILTER CIRCUITS

14.1 INTRODUCTION

The comb amplifier/filter circuits consist of the filter preamp (FP) assembly, filter (F) assembly, and the filter post-amplifier (FPA) assembly. It passes only the 875 MHz portion of the picket fence mixer signal to the 875 MHz mixer.

14.2 THEORY OF OPERATION

14.2.1 Filter Preamplifier Assembly

The filter preamplifier (FP) assembly amplifies the picket fence mixer output for use by the filter (F) assembly.

14.2.2 Filter Assembly

The filter (F) removes all but the 875 MHz portion of the PF mixer output signal as amplified by the filter preamp (FP) assembly. The output drives the filter post-amplifier (FPA) assembly.

14.2.3 Filter Post Amplifier Assembly

The filter post-amplifier (FPA) assembly increases the 875 MHz output signal level of the filter (F) assembly before entering the 875 MHz mixer/730 MHz BPF circuits.

14.3 SPECIFICATIONS

14.3.1 Filter Preamplifier Assembly

Operating Frequency	875 MHz.
Gain	9 dBm.
DC Supply	+6.0V at 55mA.
Connectors	Two SMA males

14.3.2 Filter Assembly

The 875 MHz bandpass filter assembly specifications are as follows:

Center Frequency	875 MHz.
Bandwidth at 2 dB pts.	2 MHz.
Rejection	90 dB @ ±9 MHz from center frequency.
Insertion Loss	6 dB maximum
Connectors	Two SMA female

14.3.3 Filter Post Amplifier Assembly

Operating Frequency	875 MHz.
Gain	9 dBm.
DC Supply	+6.0V at 55 mA.
Connectors	Two SMA males

14.4 MAINTENANCE

14.4.1 Preventive Maintenance

Preventive maintenance is not required for the filter preamp, filter and the filter post-amplifier assemblies. Normal operation is indicated by the presence of correct outputs.

14.4.2 Alignment/Calibration

Field or customer alignment of these assemblies is not advised. If realignment of the filter preamp or filter post-amplifier assemblies is required, return the appropriate assembly to the factory for service. If realignment of the filter assembly is required, return the entire instrument to the factory for service.

14.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If either the filter preamp or filter post-amplifier module has been isolated as the source of the problem, the only authorized service is exchange and factory repair of the module.

If the filter assembly has been isolated as the source of the problem, the only authorized service is to return the entire instrument to the factory for repair.

SECTION 15
875 MIXER/730 BPF CIRCUITS

15.1 INTRODUCTION

The 875 MHz mixer/730 MHz BPF circuits combine the 875 MHz portion of the picket fence mixer signal from the filter post-amplifier with the DMA output signal, then removes all but the 725 to 735 MHz signal.

15.2 THEORY OF OPERATION

15.2.1 875 MHz Amplifier/Mixer Assembly

Refer to schematic 03-004-5481. The 875 MHz signal from the comb amplifier/filter enters the 875 MHz amplifier/mixer at J30. Four series amplifiers (AR1, AR2, AR3 and AR4) provide gains of 11, 11, 10 and 9 respectively to the filter post-amplifier output signal before reaching a pad (R5, R6 and R7) that drives one input to mixer M1 at pin 8. The mixer input at pin 1 is supplied by the DMA module output (J31) through a pad (R8, R9 and R10). The output of M1 at pin 3 passes through J32 to the 725-735 MHz bandpass filter.

15.2.2 725-735 MHz Bandpass Filter Assembly

The 725-735 MHz BPF blocks all but the 725 to 735 MHz portion of the output signal from the 875 MHz amplifier/mixer. The output of this filter exits at J37 to be used as one of two inputs to the output mixer.

15.3 SPECIFICATIONS

15.3.1 875 MHz Amplifier/Mixer Assembly

The 875 MHz Amp/Mixer assembly specifications are as follows:

Input Signals	875 MHz. 140 to 150 MHz.
Output Signal	730 MHz.
Impedance	50 Ω.
DC Supply	+ 6V at 120 mA.
Connectors	Three SMA female.

15.3.2 725-735 MHz Bandpass Filter Assembly

The 725-735 MHz bandpass filter assembly specifications are as follows:

Passband	723 to 735 MHz
Insertion Loss	6 dB maximum
Stopband Loss (in addition to insertion loss).	
1. Low Frequency Skirt	– 35 dB from 625 to 200 MHz.
2. High Frequency Skirt	– 80 dB from 870 to 910 MHz.
Impedance	50 Ω.
Connectors	Two SMA female.

15.4 MAINTENANCE

15.4.1 Preventive Maintenance

Preventive maintenance is not required for the 875 MHz Amp/Mixer or the 725-735 MHz bandpass filter assemblies. Normal operation is indicated by the presence of correct outputs.

15.4.2 Alignment/Calibration

No alignment or calibration is necessary after replacement of individual parts.

15.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If either the 875 MHz Amp/Mixer or the 725-735 MHz bandpass filter assembly has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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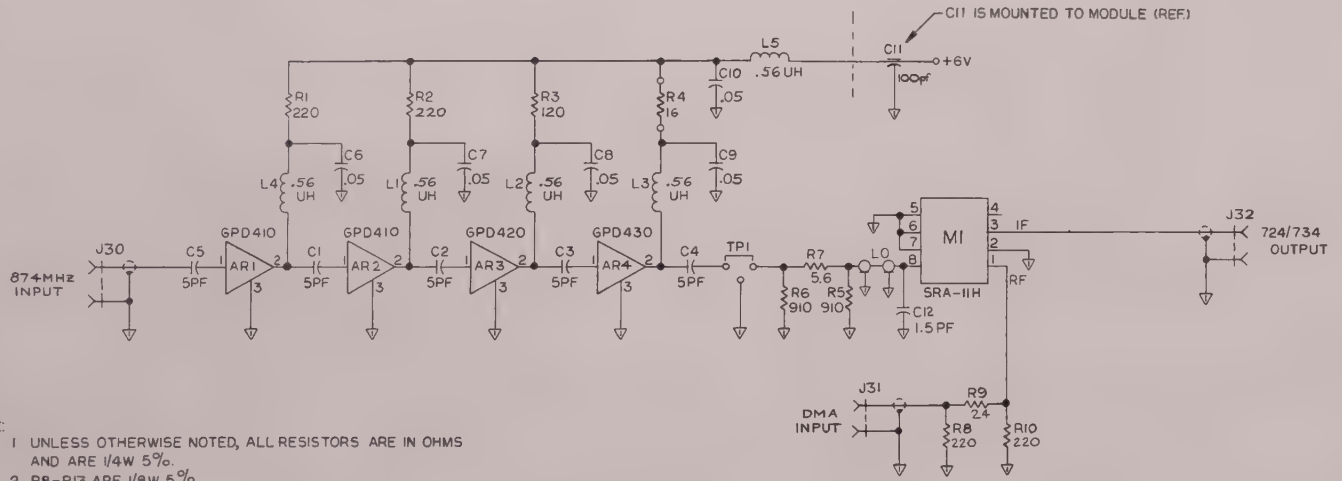
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE		RAS GV	11/1/83
	B	ECO# 1706		ESH GV	7/6/84
	C	1879	a.m. 8/23/84	ESH	5/14/85
	D	1993	M.McMINN	RAS	8/6/85

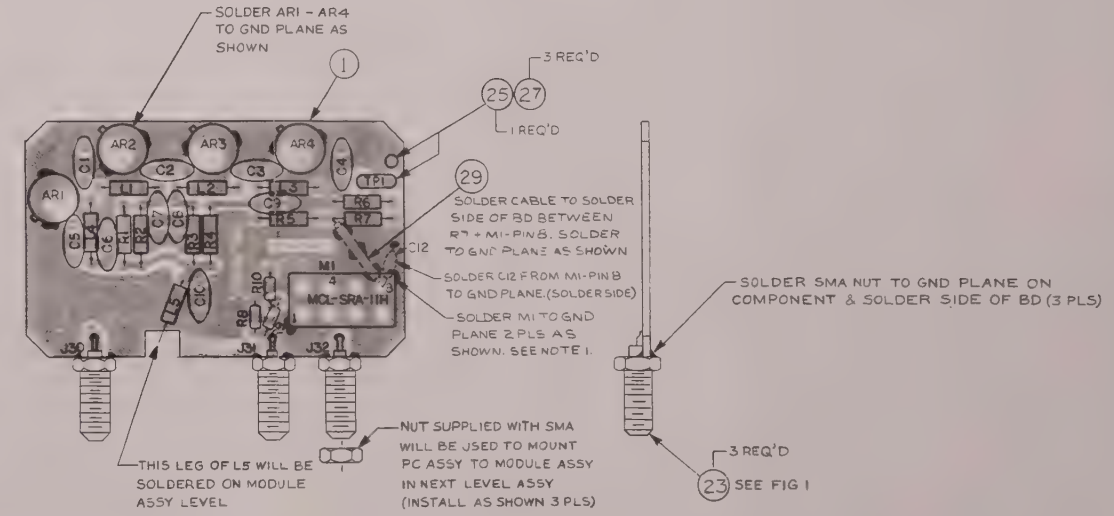


NOTE:
1. UNLESS OTHERWISE NOTED, ALL RESISTORS ARE IN OHMS AND ARE 1/4W 5%.
2. R8-R13 ARE 1/8W 5%.
3. UNLESS OTHERWISE NOTED, ALL CAPS ARE IN UF.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
x/x ±1/64 | .xxx ±.005 | .xx ±.01 | ∠ ±1°	DRAWN M.McMINN DATE 5-3-83	TITLE: ELECTRICAL SCHEMATIC 875 AMP – MIXER MODULE
MATERIAL: —	CHKD RA 11/1/83	
FINISH: —	ENG APPR. RAS 11/1/83	
	MFG APPR. GV 11/1/83	SIZE C | MODEL NO. 5150 | DRAWING NO. 03 004 5481 | REV D
	ISSUED	SCALE: — | CODE IDENT 30621 | SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED WITHOUT WRITTEN AUTHORIZATION. FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			11/1/83
	B	1706			1/24/84
	C	1861			7/24/84
	D	1879			7/24/84
	E	1908			11/20/84
	F	1993	M. McMINN		8/6/85



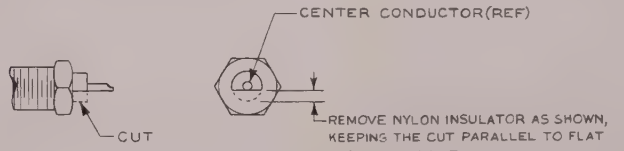


FIG 1

NOTE:
1: PIN 4 OF SRA-11H SHOULD BE CUT FLUSH WITH MIXER BEFORE INSTALLATION

SHEET 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
XX ± 1/64 XXX ± .005 XX ± .01 ∠ ± 1°
MATERIAL: N
FINISH: N

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

DRAWN	L. Peters	9/24/83
CHKD		11/1/83
ENG APPR		11/1/83
MFG APPR		11/1/83
ISSUED		

WAVETEK ROCKLAND Wavetek Rockland, Inc.

TITLE: PC ASSY 875 MHz AMP/MIXER

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5481	F

SCALE 2:1 CODE IDENT 50621 SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5481 REV F

PC ASSY: 875 MHZ AMP/MIXER

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: 874MHZ AMP/MIXER, 5150	320.5481	1.00
3	AR1,AR2	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7410	2.00
4	AR3	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7420	1.00
5	AR4	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7430	1.00
6	M1	U: DBL BAL MIXER (SRA-11H)	129.5007	1.00
8	R1,R2	R: FX CFLM 220 OHM 5% 1/4W	116.1221	2.00
9	R3	R: FX CFLM 120 OHM 5% 1/4W	116.1121	1.00
10	R4	R: FX CFLM 16 OHM 5% 1/4W	116.0161	1.00
11	R5,R6	R: FX CFLM 910 OHM 5% 1/4W	116.1911	2.00
12	R7	R: FX CFLM 5.6 OHM 5% 1/4W	116.9561	1.00
13	R8,R10	R: FX CFLM 220 OHM 5% 1/8W	116.1220	2.00
14	R9	R: FX CFLM 24 OHM 5% 1/8W	116.0240	1.00
16	C12	C: FX CER 1.5PF .5PF NPO 500V	100.9158	1.00
18	C1,C2,C3,C4,C5	C: FX CER 5.0PF .25PF NPO 500V	100.9509	5.00
19	C6,C7,C8,C9,C10	C: FX CER .05UF +20-80 Y5F 12V	100.3502	5.00
21	L1,L2,L3,L4,L5	L: FXD .56 UHY +/-10% MINI.	150.8561	5.00
23	J30,J31,J32	CONN: SMA BULK RECPT .5"	351.0023	3.00
25	TP1	PLUG: SHORTING (LOW PROF)	352.0202	1.00
27	XTP1	SOCKET: JUMPER	353.0103	3.00
29	6"	CABLE: SEMI RIGID	009.9584	1.00

SECTION 16
OUTPUT MIXER CIRCUIT

16.1 INTRODUCTION

The Output Mixer (OM) circuit combines the 725 to 735 MHz bandpass filter output signal with the 735 to 1225 MHz voltage controlled oscillator signal from the distribution amplifier. The output is fed to the 500 MHz amplifier/filter.

16.2 THEORY OF OPERATION

16.2.1 Output Mixer

Refer to schematic 03-004-5482. The pad (R9, R10 and R11) attenuates the 725 to 735 MHz bandpass filter output before entering mixer M1. The second mixer input originates from the 735 to 1225 distribution amplifier through J36. This signal is attenuated by a pad consisting of R1, R7 and R8, then amplified by AR1 and AR2. It then enters a pad (R4, R5 and R6) that drives the second input of M1 at pin 8. The resulting output signal can be any frequency less than 500 MHz. This signal passes through a pad (R12, R13 and R14) before driving the 500 MHz amplifier/filter via J38.

16.3 SPECIFICATIONS

Input Signals	725 to 735 MHz.
	735 to 1225 MHz.
Output Signal	1 to 500 MHz.
DC Supply	+6.0V at 90 mA.
Connectors	Three SMA female.

16.4 MAINTENANCE

16.4.1 Preventive Maintenance

Preventive maintenance is not required for the output mixer assembly. Normal operation is indicated by the presence of correct outputs.

16.4.2 Alignment/Calibration

No alignment or calibration is necessary after replacement of individual parts. Field or customer alignment of the output mixer assembly is not feasible nor advised. If realignment is required, return the entire instrument to the factory for service.

16.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If the output mixer assembly has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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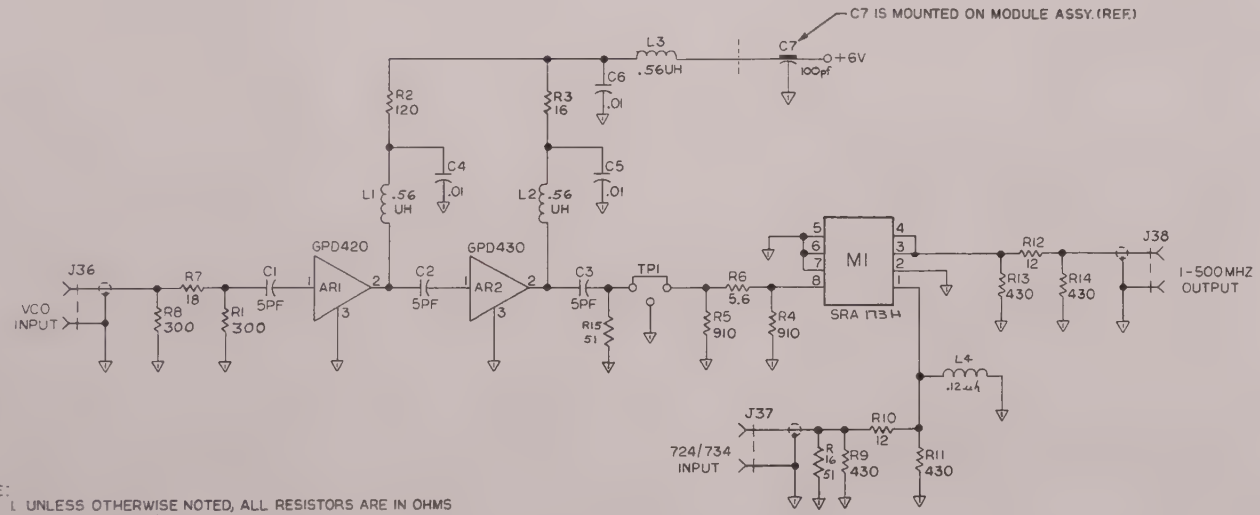
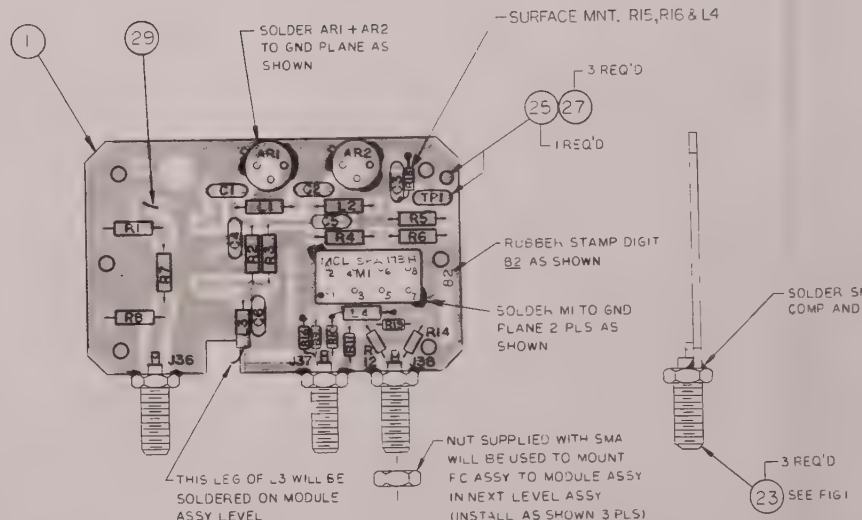
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			1/1/83
	B	ECO#1706			7/7/84
	C	ECO#1878	SR 8-27-87		9/1/4
	D	ECO 1916	SR 11/15/88		11/15/88



NOTE:
1. UNLESS OTHERWISE NOTED, ALL RESISTORS ARE IN OHMS AND ARE 1/4W 5%.
2. R9-R14 ARE 1/8W 5%.
3. UNLESS OTHERWISE NOTED, ALL CAPS ARE IN UF.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE x/x ±1/64 · .xxx ±.005 · .xx ±.01 · ∠ ±1° MATERIAL: — FINISH: —	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES DRAWN M. McMINN 5-3-83 CHKD 11/1/83 ENG APPR. 11/1/83 MFG APPR. 11/1/83 ISSUED	WAVETEK ROCKLAND — Wavetek Rockland, Inc. TITLE: ELECTRICAL SCHEMATIC OUTPUT MIXER SIZE C · MODEL NO 5150 · DRAWING NO 03-004-5482 · REV D SCALE: — · CODE IDENT 50621 · SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B				
	C				
	D				



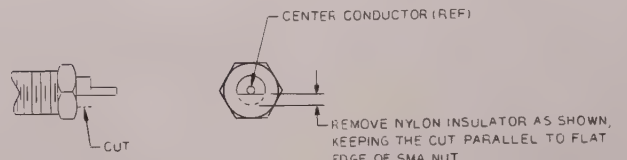


FIG 1

SHEET 2 IS "A" SIZE L/M

DR M. McMINN	DATE 9/12/83
CHKD	
ENG	
MFG	
ISSUED	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

X/64	XXX	XX	ANG
± 1/64	± .005	± .01	± 1°

MAT

FIN

WAVETEK ROCKLAND Wavetek Rockland, Inc.

PC ASSY
OUTPUT MIXER

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5482	C

SCALE 2:1 | CODE IDENT 50521 | SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5482 REV D

PC ASSY: OUT MIXER 0.1-500MHZ

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: VCO-PF/.1-500 OUT MIXER	320.5485	1.00
4	AR1	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7420	1.00
5	AR2	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7430	1.00
6	M1	U: DBL BAL MIXER (SRA173H)	129.5006	1.00
8	R1,R8	R: FX CFLM 300 OHM 5% 1/4W	116.1301	2.00
9	R2	R: FX CFLM 120 OHM 5% 1/4W	116.1121	1.00
10	R3	R: FX CFLM 16 0HM 5% 1/4W	116.0161	1.00
11	R4,R5	R: FX CFLM 910 OHM 5% 1/4W	116.1911	2.00
12	R6	R: FX CFLM 5.6 OHM 5% 1/4W	116.9561	1.00
13	R7	R: FX CFLM 18 OHM 5% 1/4W	116.0181	1.00
14	R15,R16	R: FX CFLM 51 OHM 5% 1/8W	116.0510	2.00
15	R9,R11,R13,R14	R: FX CFLM 430 OHM 5% 1/8W	116.1430	4.00
16	R10,R12	R: FX CFLM 12 OHM 5% 1/8W	116.0120	2.00
18	C1,C2,C3	C: FX CER 5.0PF .25PF NPO 500V	100.9509	3.00
19	C4,C5,C6	C: FX MONO .01UF +80 -20% 50V	100.3105	3.00
21	L1,L2,L3	L: FXD .56 UHY +/-10% MINI.	150.8561	3.00
22	L4	L: FXD .12 UHY +/-10% MINI.	150.8120	1.00
23	J36,J37,J38	CONN: SMA BULK RECPT .5"	351.0023	3.00
25	TP1	PLUG: SHORTING (LOW PROF)	352.0202	1.00
27	FOR TP1	SOCKET: JUMPER	353.0103	3.00
29	0.25"	WIRE: BUSS HD DWN TND #20 AWG	378.0500	1.00

SECTION 17
500 MHz AMPLIFIER/FILTER CIRCUITS

17.1 INTRODUCTION

The 500 MHz amplifier/filter circuits consist of 2 separate filters and a filter/amplifier. Together, they amplify and filter the output mixer signal for use by the automatic gain control circuit.

17.2 THEORY OF OPERATION

17.2.1 Low Pass Filter 1

The 500 MHz dual tuned circuits of the first low pass filter effectively block all signals above 500 MHz that originate from the output mixer. This leaves only the programmed frequency to enter the amplifier/500 MHz low pass filter.

17.2.2 Amplifier/Low Pass Filter

Refer to schematic 03-004-5472. The signal from the 500 MHz low pass filter enters the amplifier/500 MHz low pass filter through J40. This signal is filtered by an additional series-tuned circuit before being amplified by AR1 and AR2. The signal is attenuated by a 5 dB pad before being amplified by AR3.

A roving frequency spur is eliminated by the variable notch filter consisting of C20, R14, L7 and CR1. For each frequency programmed by the front panel or remote bus, the frequency of this spur has been calculated by the front panel circuitry. A tuning voltage from the front panel is varied at one end of C20 to keep pace with the frequency of this spur. After passing through the variable notch filter, the desired signal is amplified by AR4, then attenuated 2 dB by a pad consisting of R8, R9 and R10, and filtered by L5 and C11. Another 10 dB of attenuation is provided by R11, R12 and R13 before reaching the output at J41.

17.2.3 Low Pass Filter 2

The 500 MHz low pass filter is identical to the filter described in paragraph 17.2.1. It uses a dual tuned low pass filter to eliminate all signals above 500 MHz from the amplifier/500 MHz low pass filter output signal. The output of this circuit, at 50Ω impedance, drives the AGC circuitry.

17.3 SPECIFICATIONS

17.3.1 Low Pass Filter 1

Frequency Cutoff	540 MHz minimum to 580 MHz maximum.
Stopband Loss	⩽ – 45 dBc min at 725 MHz.
Impedance	50Ω.
Connectors	Two SMA male.

17.3.2 Amplifier/Low Pass Filter

Module Gain	+ 32 dB ± 2 dBm.
Frequency Cutoff	525 MHz minimum to 550 MHz maximum.
Stopband Loss	⩽ – 30 dBc min at 725 MHz.
Impedance	50Ω.
DC Supply	+ 6.0V at 280 mA.
Connectors	Two SMA female.

17.3.3 Low Pass Filter 2

Frequency Cutoff	540 MHz minimum to 580 MHz maximum.
Stopband Loss	⩽ – 45 dBc min at 725 MHz.
Impedance	50Ω.
Connectors	Two SMA male.

17.4 MAINTENANCE

17.4.1 Preventive Maintenance

Preventive maintenance is not required for the amplifier/filter or the low pass filter assemblies. Normal operation is indicated by the presence of correct outputs.

17.4.2 Alignment/Calibration

No alignment or calibration is necessary after replacement of individual parts on the amplifier and low pass filter circuits. Field or customer alignment of either low pass filter is not advised. If realignment is required, return the assembly to the factory for service.

17.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If the amplifier or a low pass filter has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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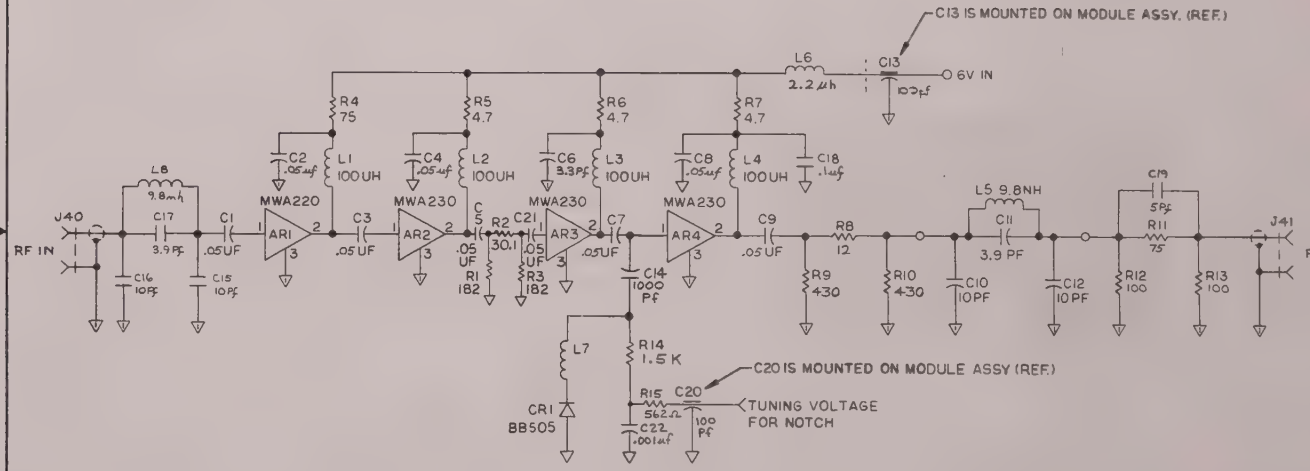
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE			11/1/83
	B	ECO# 1706	JP		1/1/84
	C	1970	M. McMINN		4/5/85
	D	2005	M. McMINN		8/22/85
	E	2078	M. McMINN		1/22/86
	F	2088	M. McMINN		5/7/86



NOTES:
1. ALL RESISTORS ARE IN OHMS AND ARE 1/8W 5% EXCEPT AS NOTED.
2. R1, R2 AND R3 ARE IN OHMS AND ARE 1/3W 1%

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
x/x ±1/64 | .xxx ±.005 | .xx ±.01 | ∠ ±1°
MATERIAL: ——
FINISH: ——

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

DRAWN	M. McMINN	DATE 7/28/83
CHKD		11/7/13
ENG APPR.		11/7/13
MFG APPR.		11/11/83
ISSUED		

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: ELECTRICAL SCHEMATIC 500MHZ LPF

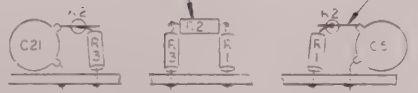
SIZE	MODEL NO.	DRAWING NO	REV
C	5150	03-004-5472	F

SCALE: — | CODE IDENT 50621 | SHEET 1 OF 1

ZONE	LTR	ECO NO.	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	ECO# 706	JF		7/-/84
	C	1676			
	D	2076			
	E	2[illegible]			

NOTE C5 AND C21 WITCH FALL DIRECTLY BEHIND R1 AND R3 ARE NOT SHOWN IN THIS VIEW FOR CLARITY

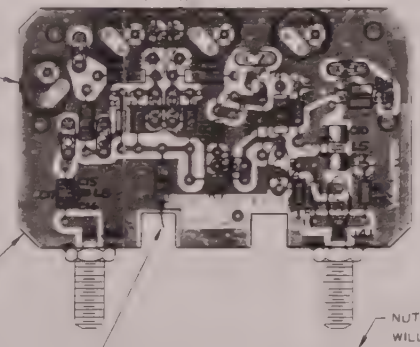
INSTALL CAP FIRST. UPPER CAP LEAD MUST BE KEPT PARALEL TO BD. USE THIS LEAD AS A WIRE POST TO WRAP RESISTOR LEADS AROUNDS. KEEP ALL COMPONENT LEADS TO MINIMUM LENGTH. (TYP C5 AND C21)



DETAIL A
ROTATED 180

C5 AND C21 ARE SHOWN MISALIGNED WITH R1 AND R3 IN THIS VIEW TO SHOW MOUNTING HOLES FOR BOTTOM LEAD OF C5 AND C21

TACK SOLDER AR1-AR4 TO GND PLANE AS SHOWN



SOLDER SMA NUT TO GND PLANE ON COMP AND SOLDER SIDE OF BD (2 PLS)

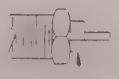
2 REQ'D
(18) SEE FIG 1

(1)

THIS LEG OF L6 WILL BE SOLDERED ON MODULE ASSY LEVEL

NUT SUPPLIED WITH SMA WILL BE USED TO MOUNT PC ASSY TO MODULE ASSY IN NEXT LEVEL ASSY (INSTALL AS SHOWN 2 PLS)

CENTER CONDUCTOR (REF)



CUT

REMOVE NYLON INSULATOR AS SHOWN, KEEPING THE CUT PARALLEL TO FLAT EDGE OF SMA NUT

FIG 1

SHEET 2 IS A" SIZE L M

DRAWN		DATE
CHKD		
ENG		
MFG		
ISSUED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

XX ±.164	XXX ±.005	XX ±.01	∠ ±1°

MAT'

FIN

WAVETEK ROCKLAND Wavetek Rockland, Inc

PC ASSY
500MHZ LPF

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02 004 5472	E

SCALE	CODE IDENT	SHEET
2:1	50E21	1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5472 REV E

PC ASSY: 500 MHZ LPF

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: 500MHZ LPF MODULE, 5150	320.5472	1.00
3	AR1	U: WIDE BAND HYB AMP DC-600MHZ	120.7220	1.00
4	AR2,AR3,AR4	U: WIDE BAND HYB AMP DC-600MHZ	120.7230	3.00
5	R12,R13	R: FX MFLM 100 OHM 1% 1/8W T0	110.1000	2.00
6	R8	R: FX CFLM 12 OHM 5% 1/8W	116.0120	1.00
7	R9,R10	R: FX CFLM 430 OHM 5% 1/8W	116.1430	2.00
8	R4,R11	R: FX CFLM 75 OHM 5% 1/8W	116.0750	2.00
9	R5,R6,R7	R: FX CFLM 4.7 OHM 5% 1/8W	116.9470	3.00
10	R14	R: FX MFLM 1.50K 1% 1/10W T2	111.1501	1.00
11	C1,2,3,4,5,7,8,9,21,	C: FX CER .05UF +20-80 Y5F 12V	100.3502	9.00
12	C10,C12,C16,C15	C: FX CER CHIP 10PF	107.0102	4.00
13	C11,C17	C: FX CER CHIP 3.9PF	107.9392	2.00
14	C19	C: FX CER 5.0PF .25PF NPO 500V	100.9509	1.00
15	L1,L2,L3,L4	L: FXD 100 UHY +/-10% MINI.	150.1101	4.00
16	L5,L8	L: TOROID, 3 TURN, (T7/36AWG)	012.1060	2.00
17	L6	L: FXD 2.2 UHY +/-10% MINI.	150.9221	1.00
18	J40,J41	CONN: SMA BULK RECPT .5"	351.0023	2.00
19	C18	C: FX CER .1UF +80 -20% 12V	100.4100	1.00
20	C14	C: FX CER CHIP 1000PF	107.2102	1.00
21	C6	C: FX CER 3.3PF .5PF NPO 500V	100.9338	1.00
22	6"	WIRE: BUSS TINNED #16 AWG	378.0300	1.00
24	L7	L: TOROID,4TURN,{T16/30AWG}	012.1062	1.00
26	CR1	CR: VARACTOR (BB505B)	133.0105	1.00
28	R2	R: FX MFLM 30.1 OHM 1% 1/3W	119.3015	1.00
29	R1,R3	R: FX MFLM 182 OHM 1% 1/3W	110.1825	2.00

SECTION 18
AUTOMATIC GAIN CONTROL CIRCUIT

18.1 INTRODUCTION

The Automatic Gain Control (AGC) circuit reduces amplitude variations (amplitude change with frequency) originating from the 500 MHz amplifier/filter. This provides a more stable output amplitude from the instrument throughout the entire frequency range. The AGC output drives the frequency doubler and bandswitch 0 and 1 circuits.

18.2 THEORY OF OPERATION

Refer to schematic 03-004-5480. The 1 to 500 MHz signal at J45 from the 500 MHz amplifier/filter is attenuated by R1, R2 and R3. Amplifier U2 provides a 10 dB gain before the signal reaches the voltage controlled attenuator circuit consisting of CR1, CR2 and CR3. As explained in the following paragraphs, the VCA acts as a continuously variable attenuator, with the amount of attenuation being directly proportional to the signal amplitude at U5 pin 7, which is fed back to the VCA via U1. U3 amplifies the VCA output by 10 dB, and power splitter U5 provides an amplitude stable input to the frequency doubler (J47) and bandswitch 0 and 1 (J46) circuits, as well as providing the VCA feedback.

As the voltages at the anodes of CR1, CR2 and CR3 increase, the diodes' resistance to the RF signal also increases. Because CR1 and CR3 are in series with the RF signal, an increase in resistance of these diodes means a decrease in the RF signal level at U3 pin 1. With CR2 in parallel with the RF signal, a decrease in resistance of this diode causes a decrease in the RF signal level at U3 pin 1 because the RF signal is shunted to ground through C5.

As the voltage at U5 pin 7 decreases, the voltage at U1 pin 9 also decreases. This increases the voltage at pin 8, forward biasing CR2 (which provides a parallel path through C5 for the RF signal) and decreasing the voltage at U1 pin 14. A more negative voltage is now seen at the anodes of both CR1 and CR3, increasing their resistance to the RF signal.

18.3 SPECIFICATIONS

Input Signal	1 to 500 MHz (from LPF2).
Output Signals	1 to 500 MHz (to BDSW 0 & 1). 1 to 500 MHz (to DOUBLER).
DC Supply	−12.4V at 8 mA. +28V at 16 mA. +6.0V at 105 mA.
Connectors	Three SMA female.

18.4 MAINTENANCE

18.4.1 Preventive Maintenance

Preventive maintenance is not required for the AGC module. Normal operation is indicated by the presence of correct outputs.

18.4.2 Alignment/Calibration

Field or customer alignment of the AGC module is not advised. If realignment is required, return the assembly to the factory for service.

18.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If the AGC module has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	B	RELEASE		BRS	11/6/84
	C	920		DS	5/3/84
	D	922		DS	5/23/84
	E	1969	M. McMinn		

0.1-500 MHZ
(FROM IN-LINE 500 MHZ) J45
LPF #2

R2 12Ω 1/8W 5%
R3 430Ω 1/8W 5%
C2 .05 UF
U2 MWA 230
RF AMPLIFIER
C3 .05 UF
CR1
L2 100 UH
C4 1000 UF
L4 100 UH
C5 1000 UF
CR2
L3 100 UH
CR3
C6 .05 UF
L5 100 UH
C7 1000 UF
U3 MWA-230
RF AMPLIFIER
C9 .05 UF
+6VDC
R4 18Ω 1/8W 5%
C1 .05 UF
L1 100 UH
+6VDC
R5 18Ω 1/8W 5%
C8 .05 UF
L6 100 UH
VOLTAGE CONTROLLED ATTENUATOR

U5
PSC3-1W
3-WAY POWER SPLITTER
CR4 HSCH-3486
R9 100K
C10 .01
RF DETECTOR

0.1-500 MHZ
J46 (TO BANDSWITCH Ø AND I)
J47 (TO DOUBLER)

-5 VDC
R18 162K
R29 100K RND
+28 VDC
R28 150K
-12 VDC
LF347 U1
R19 1K
R20 10K
C11 22PF
R17 1K
R22 10K
CR5
TEMPERATURE COMPENSATION
0-12VDC

LINEARIZER
R23 11K
R16 33.2Ω
C18 0.1 UF
R15 274K
R10 1K
R21 150K
R25 243K
R26 1K
R24 100K
TP1
R13 5.62K
LF347 U1
DC AMPLIFIER
R11 100K
LF347 U1
INTEGRATOR
R27 100K

+12VDC
R12 10K
R14 10K RND
R8 10K
-12VDC

NOT PART OF THIS ASSY.

+28 VDC
C17 .00 PF
LM78L12AC U4
+12 VDC
C12 0.1 UF 50V
C13 .05 UF 25V

+6VDC
C15 100 PF
L7 100 UH
+6 VDC

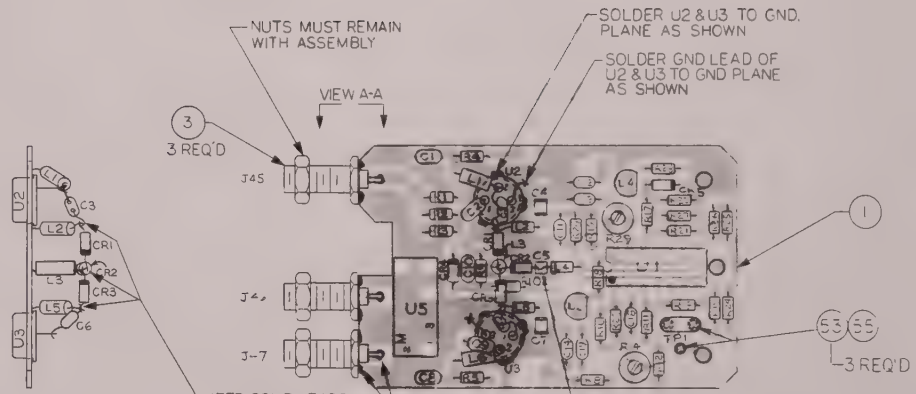
-12 VDC
C16 100 PF
LM79L05AC U6
-5 VDC
C14 .05 UF 25V
C19 .05 UF 12V

NOTES:
1. ALL DIODES ARE HP5082-3080 UNLESS OTHERWISE NOTED.
2. ALL RESISTORS ARE 1/3W 1% UNLESS OTHERWISE NOTED.

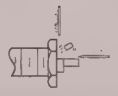
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES
DRAWN M. McMinn 5/24/85
CHK'D
ENG APPR 5/14 12/2/85
MFG APPR
ISSUED
MATERIAL
FINISH

WAVETEK Wavetek Inc.
TITLE ELECTRICAL SCHEMATIC AGC
SIZE D MODEL NO 5150 DRAWING NO 03-004-5480 REV E
SCALE — CODE IDENT 23338 SHEET OF

ZONE	LTR	ECO NO.	CHANGED BY	APPR'D BY	DATE
	B	RELEASE			
	E	1969	M. McMINN		



VIEW A-A



SMA ALTERATION

CUT RIGHT ANGLE NOTCH OUT OF TEFLON WITH EXACTO KNIFE AS SHOWN. PLACE SMA ON P.C. WITH THE NOTCH DOWN ON COMP. SIDE.
NOTE: SMA'S MUST BE CENTERED ON P.C. LANDS. USE FIXTURE TO MOUNT SMA'S.
(SOLDER AS DESCRIBED ABOVE)

SHEET 2 & 3 ARE "A" SIZE L/M

DR		DATE
CHKD		
ENG		
MFG		
ISSUED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
XX ± .005 | XXX ± .010 | ANG ± 1°
MAT'L
FIN

WAVETEK ROCKLAND Wavetek Rockland, Inc.

P.C. ASSEMBLY
A.G.C.

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5480	E
SCALE 2:1	CODE IDENT 50621	SHEET 1 OF 3	

WAVETEK SD INC. DWG NO. 02 004 5480 REV E

PC ASSY: AGC MODULE

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: AGC MODULE, 5150	320.5480	1.00
3	-	CONN: SMA BULK RECPT .5"	351.0023	3.00
5	U1	U: QD LIN BIFET OP-AMP (LF347)	120.2047	1.00
6	U5 (PSC3-1W)	U: PWR SPLTR, 3WAY 5MHZ-500MHZ	129.6002	1.00
7	U2,U3	U: WIDE BAND HYB AMP DC-600MHZ	120.7230	2.00
9	U4	Q: P.V. REG 12V TO-92 (78L12C)	120.0122	1.00
10	U6	Q: N.V. REG 5V (79L05)	120.0054	1.00
12	R1,R3	R: FX CFLM 430 OHM 5% 1/8W	116.1430	2.00
13	R2	R: FX CFLM 12 OHM 5% 1/8W	116.0120	1.00
14	R4,R5,	R: FX CFLM 18 OHM 5% 1/8W	116.0180	2.00
15	R9	R: FX CFLM 100K OHM 5% 1/8W	116.4100	1.00
16	R10	R: FX CFLM 1.0K OHM 5% 1/8W	116.2100	1.00
19	R11,R24,R27,	R: FX MFLM 100.0K OHM 1% 1/3W	113.1005	3.00
20	R8,R12,R20,R22,	R: FX MFLM 10.0K OHM 1% 1/3W	112.1005	4.00
21	R13,	R: FX MFLM 5.62K OHM 1% 1/3W	111.5625	1.00
22	R15,	R: FX MFLM 27.4K OHM 1% 1/3W	112.2745	1.00
23	R16,	R: FX MFLM 33.2 OHM 1% 1/3W	119.3325	1.00
24	R17,R19,R26	R: FX MFLM, 1.00K 1% 1/3W T0	111.1005	3.00
25	R18,	R: FX MFLM 162.0K OHM 1% 1/3W	113.1625	1.00
26	R21,	R: FX MFLM 150.0K OHM 1% 1/3W	113.1505	1.00
27	R23,	R: FX MFLM 11.0K OHM 1% 1/3W	112.1105	1.00
28	R25,	R: FX MFLM 243.0K OHM 1% 1/3W	113.2435	1.00
29	R28,	R: FX MFLM 150.0K OHM 1% 1/3W	113.1505	1.00
32	R14,	R: VAR CMT 10K 1/4" RND	118.3100	1.00
33	R29,	R: VAR CMT 100K 1/4" RND	118.4101	1.00
35	C1,C2,C3,C6,C8,C9,C19,	C: FX CER .05UF +20-80 Y5F 12V	100.3502	7.00
37	C4,C5,C7,	C: FX CER CHIP 1000PF	107.2102	3.00
39	C10,	C: FX CER .01UF +80 -20% 50V	100.3101	1.00
41	C11,	C: FX MICA DP 22PF +-5% 500V	101.0220	1.00
43	C12,C18,	C: FX MONO 0.1UF Z5U 50V	100.4102	2.00
45	C13,C14,	C: FX CER .05UF 20% Y5P 25V	100.3501	2.00
47	CR1,CR2,CR3,CR5,	CR: PIN (5082-3080)	133.3080	4.00
49	CR4 (HSCH-3486 D/C 317A)	CR: DETECTOR	133.3486	1.00
51	L1-L6,	L: FXD 100 UHY +/-10% MINI.	150.1101	6.00
53	TP1,TP2,TP3,	SOCKET: JUMPER	353.0103	3.00
55	-	PLUG: SHORTING (LOW PROF)	352.0202	1.00

SECTION 19
FREQUENCY DOUBLER

19.1 INTRODUCTION

The Frequency Doubler (FD) makes available the programmed output frequencies between 500 and 1000 MHz. It doubles the 1 to 500 MHz automatic gain control output frequency for use by the bandswitch 2 (500 to 750 MHz) and bandswitch 3 (750 to 1000 MHz) circuits.

19.2 THEORY OF OPERATION

Refer to schematic 03-004-5470. The frequency doubler receives the 1 to 500 MHz RF signal from the automatic gain control circuit at J48. This signal is input to amplifier U1 which has a gain of 10 dB. As explained in the following paragraphs, an RF switch (CR1, CR2, and CR3) controlled by the TTL input from the front panel (via Q1 and Q2) blocks the RF signal if the programmed frequency is less than 500 MHz. If the programmed frequency is greater than 500 MHz, the signal passes through the RF switch and a pad before reaching the frequency doubling circuit, U2. Amplifiers U3 and U4 at the output of U2 each increase the signal strength by approximately 10 dB before it reaches resistive power splitter R12, R13 and R14. The outputs drive bandswitch 2 (J49) and bandswitch 3 (J50).

When the voltage at the junction of CR1, CR2 and CR3 is low, the RF signal attenuation is at maximum. Because CR1 and CR3 are in series with the RF signal, maximum resistance of these diodes provides a virtual cutoff of the RF signal level at TP1. In addition, with CR2 in parallel with the RF signal, minimum resistance of this diode further reduces the RF signal level by shunting it to ground.

When TTL (at the base of Q1) goes high, the voltage at the base of Q2 goes low, increasing the voltage at the collector of Q2 and the junction of CR1, CR2 and CR3. This forward biases CR1 and CR3, providing minimum resistance to the RF signal. It also reverse biases CR2, providing maximum resistance to the RF signal. Conversely, when TTL goes low, the voltage at the junction of CR1, CR2 and CR3 also goes low, reversing the previous condition, effectively chocking off the RF signal.

19.3 SPECIFICATIONS

Input Signal	1 to 500 MHz.
Output Signal	500 to 1000 MHz.
DC Supply	−12.4V at 15 mA.
	+6.0V at 120 mA.
Connectors	Three SMA female.

19.4 MAINTENANCE

19.4.1 Preventive Maintenance

Preventive maintenance is not required for the doubler module. Normal operation is indicated by the presence of correct outputs.

19.4.2 Alignment/Calibration

No alignment or calibration is necessary after replacement of individual parts.

19.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If the doubler has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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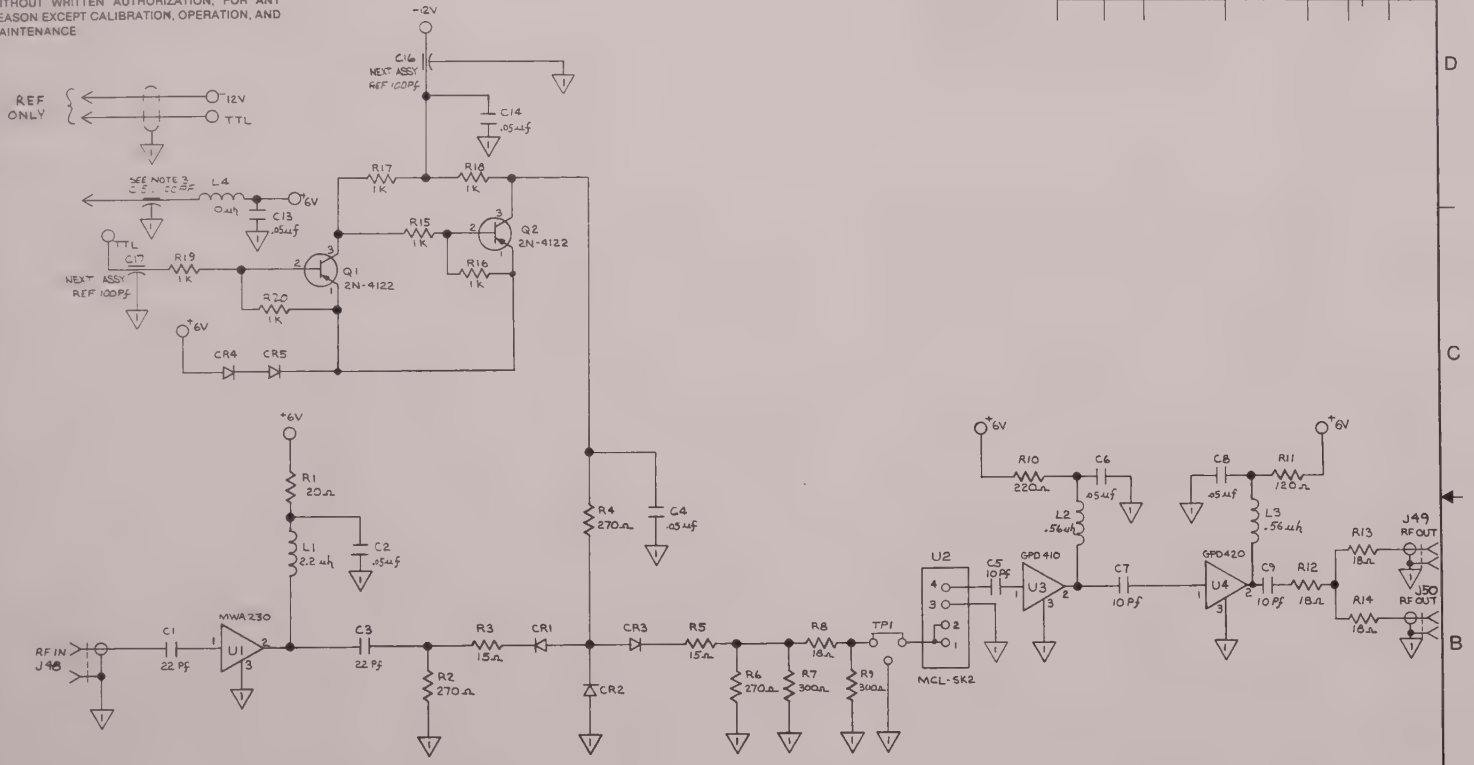
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	B	RELEASE		RDS	7/1/83
	C	ECO# 1706		RDS	7/2/84

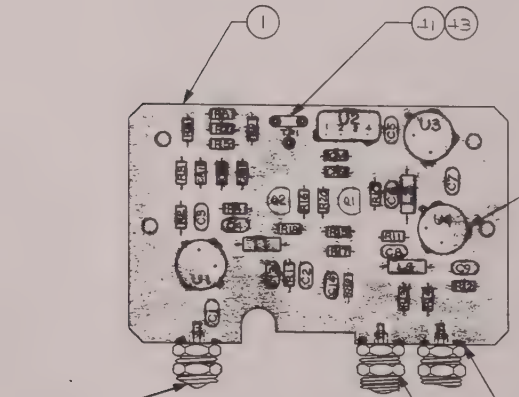


NOTES:

1. ALL R's ARE 1/8W 5%
2. ALL DIODES ARE KS3542 (PIN)
3. NOT INSTALLED ON 004-LEVEL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
x/x ±1/64 .xxx ±.005 .xx ±.01 ±1°	DRAWN JP DATE 8-3-83	TITLE: SCHEMATIC DOUBLER
MATERIAL:	CHKD [illegible] 11/1/83	
FINISH:	ENG APPR RDS 11/1/83	SIZE C MODEL NO 5150 DRAWING NO. 03-004-5470 REV C
	MFG APPR. [illegible] 11/1/83	SCALE NONE CODE IDENT 50621 SHEET 1 OF 1
	ISSUED	

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	C	RELEASE		JSA	11-1-83
	D	ECO# 1706			2/3/84
	E	1998	M. McMINN		8/5/85



3 PLACES

SOLDER U1, U2, U3, AND U4 TO P.C. GROUND PLANE IN 3 PLS. AT APPROX. LOCATIONS AS SHOWN

SOLDER EACH SMA 5 PLS. CENTER CONTACT TO LAND, EACH SIDE OF HEX TO GND. PLANE ON COMP. & SOLDER SIDE (USE FIXTURE TO MOUNT SMA'S)

NUTS MUST REMAIN WITH ASSEMBLY (DO NOT TIGHTEN)

"SMA" ALTERATION

CUT RIGHT ANGLE NOTCH OUT OF TEFLON WITH EXACTO KNIFE AS SHOWN. PLACE SMA ON P.C. WITH THE NOTCH DOWN ON THE P.C. SOLDER IN PLACE AS SHOWN ABOVE. CAUTION- SMA'S MUST BE CENTERED ON P.C. LANDS. (USE FIXTURE TO MOUNT SMA'S)

DR JP	DATE 7-27-83
CHKD	
ENG.	11/1/83
MFG.	11/1/83
ISSUED	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/64 ± 1/64	xxx ± .005	xx ± .01	∠ ± 1°

MAT

FIN

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

P.C. ASSEMBLY DOUBLE

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5470	E

SCALE 2:1 | CODE IDENT 50621 | SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5470 REV E

PC ASSY: DOUBLER

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: DOUBLER MODULE, 5150	320.5470	1.00
2	U2	DOUBLER	129.5100	1.00
3	U1	U: WIDE BAND HYB AMP DC-600MHZ	120.7230	1.00
5	U3	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7410	1.00
7	U4	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7420	1.00
9	Q1,Q2	Q: SIL PNP (2N4122)	136.4122	2.00
11	CR1 THRU CR5	CR: PIN	133.3542	5.00
13	C2,C4,C6,C8,C13,C14	C: FX CER .05UF +20-80 Y5F 12V	100.3502	6.00
15	C5,C7,C9	C: FX CER 10PF 5% NPO 500V	100.0109	3.00
17	C1,C3	C: FX CER 22PF 5% NPO 500V	100.0229	2.00
19	R3,R5	R: FX CFLM 15 OHM 5% 1/8W	116.0150	2.00
21	R12,R13,R14,R8	R: FX CFLM 18 OHM 5% 1/8W	116.0180	4.00
22	R1	R: FX CFLM 20 OHM 5% 1/8W	116.0200	1.00
23	R11	R: FX CFLM 120 OHM 5% 1/8W	116.1120	1.00
25	R10	R: FX CFLM 220 OHM 5% 1/8W	116.1220	1.00
27	R2,R4,R6	R: FX CFLM 270 OHM 5% 1/8W	116.1270	3.00
29	R7,R9	R: FX CFLM 300 OHM 5% 1/8W	116.1300	2.00
31	R15 THRU R20	R: FX CFLM 1.0K OHM 5% 1/8W	116.2100	6.00
33	L1	L: FXD 2.2 UHY +/-10% MINI.	150.9221	1.00
37	L2,L3	L: FXD .56 UHY +/-10% MINI.	150.8561	2.00
39	-	CONN: SMA BULK RECPT .5"	351.0023	3.00
41	-	SOCKET: JUMPER	353.0103	3.00
43	-	PLUG: SHORTING (LOW PROF)	352.0202	1.00

SECTION 20
BANDSWITCHING CIRCUITS

20.1 INTRODUCTION

The three bandswitching circuits select the proper RF signal path between the automatic gain control and voltage controlled attenuator circuits. Each bandswitch covers a different frequency range. Bandswitch 0 and 1 passes the 1 to 500 MHz signal between the AGC and summer module. For frequencies between 500 and 750 MHz, bandswitch 2 routes the signal from the frequency doubler to the 500-750 MHz bandpass filter. Bandswitch 3 routes the 750 to 1000 MHz signal from the frequency doubler to the 500-750 MHz bandpass filter. The output of all three bandpass filters are input to the summer module. For any programmed frequency, two bandswitches will always block the RF signal while the third passes it to the summer module.

20.2 THEORY OF OPERATION

20.2.1 Bandswitch 0 and 1

Refer to schematic 03-004-5451. Bandswitch 0 and 1 receives the 1 to 500 MHz AGC output. This signal at J51 is input to amplifier AR1 through a 7 dB pad (R7, R8 and R9). Two sets of RF switches (CR3, CR4, CR5 and CR6, CR7, CR8) controlled by the TTL input from the front panel via Q1 blocks the RF signal if the programmed frequency is greater than 500 MHz.

When the control voltage to RF switch 1 (the junction of CR3 and CR4) and RF switch 2 (the junction of CR6 and CR7) is high, the RF signal is effectively cut off. Because CR3, CR5, CR6 and CR8 are in series with the RF signal, maximum resistance of these diodes greatly attenuates the RF signal level before reaching the output at J52. In addition, with CR4 and CR7 in parallel with the RF signal, minimum resistance of these diodes decreases the RF signal level by shunting it to ground.

When the voltage at TTL (Q1 base) goes low, the junction of CR3 and CR4 goes high. This forward biases CR3 and CR5, and reverse biases CR4, providing little resistance to the RF signal. Conversely, when TTL goes high, the voltage at the junction of CR3 and CR4 goes low, reverse biasing CR3 and CR5, and forward biasing CR4, effectively chocking off the RF signal. RF switch 2 works in the same manner.

For the Model 5156A, the TTL control line originates from U52 pin 16 on the remote front panel board 004.5422. For the Model 5155A, the TTL control line originates from U47 pin 16 on the front panel board 002.5423.

The output at J52 is one of three inputs to the summer module.

20.2.2 Bandswitch 2

Refer to schematic 03-004-5452. Bandswitch 2 receives the 1 to 1000 MHz frequency doubler circuit output. This RF signal, at J55, is input to amplifier AR1 through a pad (R1, R2 and R3). As explained in the following paragraphs, when the programmed frequency is below 560 MHz, the TTL control line remains high, and Q2 causes bandswitch 1 (CR3, CR4 and CR5) to block the RF signal. Between 500 and 560 MHz, the TTL NOTCH control line goes low, causing Q1, through CR2, to connect the RF signal to a tuned filter (L3, L4 and C4). This filter blocks any frequency spur at, or slightly above, 750 MHz. In addition, the TTL NOTCH control line, via CR13, maintains the base of Q3 low, allowing the RF signal to pass through bandswitch 2 (CR14, CR15 and CR16) to the output at J56 where it enters the 500 to 750 MHz band pass filter. Between 560 and 750 MHz, the RF signal passes directly through both RF switches. Above 750 MHz, the TTL and TTL NOTCH control lines are both high, blocking the signal at the RF switches.

As mentioned in the previous paragraph, two sets of RF switches (CR3, CR4, CR5 and CR14, CR15, CR16) controlled by the TTL input via Q2 and Q3 are used to block the RF signal. When the control voltage to RF switch 1 (the junction of CR3 and CR4) or RF switch 2 (the junction of CR14 and CR15) is high, the RF signal is effectively cut off through that switch. Because CR3, CR5, CR14 and CR15 are in series with the RF signal, maximum resistance of these diodes greatly attenuates the RF signal level before reaching the output at J56. In addition, with CR4 and CR16 in parallel with the RF signal, minimum resistance of these diodes decreases the RF signal level by shunting it to ground.

When the voltage at TTL (Q2 base) goes low, the junction of CR3 and CR4 goes high. This forward biases CR3 and CR5, and reverse biases CR4, providing little

resistance to the RF signal. Conversely, when TTL goes high, the voltage at the junction of CR3 and CR4 goes low, reverse biasing CR3 and CR5, and forward biasing CR4, effectively chocking off the RF signal. RF switch 2 works in the same manner except that both TTL and TTL NOTCH must be high for this switch to block the signal.

For the Model 5156A, the TTL control line originates from U52 pin 12, and the TTL NOTCH control line originates from U53 pin 19 on the remote front panel board 002.5422. For the Model 5155A, the TTL control line originates from U47 pin 12, and the TTL NOTCH control line originates from U41 pin 19 on the front panel board 002.5423.

20.2.3 Bandswitch 3

Refer to schematic 03-004-5453. Except for minor circuit differences, bandswitch 3 is identical to bandswitch 0 and 1. Therefore, the bandswitch 0 and 1 circuit description applies here with the following changes:

- The input at J53 (not J51) originates from the 500 to 1000 MHz doubler circuit (not the AGC circuit).
- The output to the 750 to 1000 MHz band pass filter is at J54 (not J52).
- The two sets of RF switches block the RF signal if the programmed frequency is not between 750 and 1000 MHz.
- For the Model 5156A, the TTL control line originates from U52 pin 15 on the remote front panel board 002.5422. For the Model 5155A, the TTL control line originates from U47 pin 15 on the front panel board 002.5423.

20.2.4 Bandpass Filter Assemblies

The bandpass filters (3023 and 3024) are passive, low insertion loss (less than 6 dB) filters. Bandpass "3024" passes all frequencies between 750 and 1000 MHz from bandswitch 2 to the summer module. At 500 MHz and below, signals are attenuated at least 60 dB. At 1125 MHz and above, signals are attenuated at least 45 dB. Bandpass "3023" passes all frequencies between 500 and 750 MHz from bandswitch 3 to the summer module. At 375 MHz and below, signals are attenuated at least 55 dB. At 865 MHz and above, signals are attenuated at least 35 dB.

20.3 SPECIFICATIONS

20.3.1 Bandswitch 0 and 1

Input Signals	TTL Control. 1 to 500 MHz.
Output Signal	1 to 500 MHz.
Off Isolation	– 80 dB.
DC Supply	– 12.4V at 16 mA. + 6.0V at 28 mA.
Connectors	Two SMA female.

20.3.2 Bandswitch 2

Input Signals	TTL Control. Notch Control. 500 to 1000 MHz.
Output Signal	500 to 1000 MHz.
Off Isolation	– 80 dB.
DC Supply	– 12.4V at 32 mA. + 6.0V at 28 mA.
Connectors	Two SMA female.

20.3.3 Bandswitch 3

Input Signals	TTL Control. 500 to 1000 MHz.
Output Signal	500 to 1000 MHz.
Off Isolation	– 80 dB.
DC Supply	– 12.4V at 16 mA. + 6.0V at 28 mA.
Connectors	Two SMA female.

20.4 MAINTENANCE

20.4.1 Preventive Maintenance

Preventive maintenance is not required for the three bandswitch assemblies or the two bandpass assemblies. Normal operation is indicated by the presence of correct outputs.

20.4.2 Alignment/Calibration

No alignment or calibration is necessary after replacement of individual parts in any bandswitch assembly.

Field or customer alignment of the bandswitch and bandpass assemblies is not advised. If realignment of either bandpass assembly is required, return the appropriate assembly to the factory for service.

20.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If has been isolated as the source of the problem, the only authorized service is exchange and factory repair of the assembly.

If either bandpass assembly has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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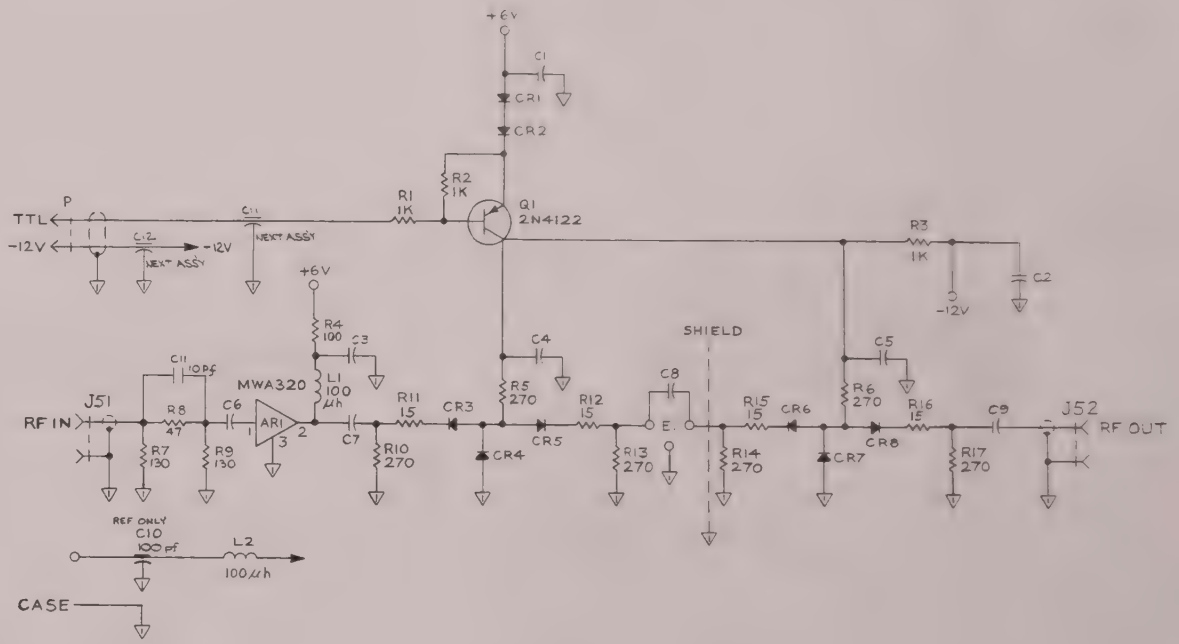

NOTE:
1. UNLESS OTERWISE SPECIFIED.
   a) ALL RESISTORS ARE IN OHMS ±5%, 1/8W.
   b) ALL CAPACITORS ARE .05µf UNLESS OTHERWISE NOTED
   c) DIODES CR1-CR5 ARE KSW3542
      CR6-CR8 ARE 5082-3060

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND — Wavetek Rockland Inc
x/x ± 1/64 · xxx ± .005 · xx ± .01 · ± 1°	DRAWN L. Peta DATE 2/83	TITLE: ELECTRICAL SCHEMATIC BANDSWITCH 0 & 1
MATERIAL:	CHKD	
FINISH	ENG APPR	
	MFG APPR	
	ISSUED	SIZE C · MODEL NO. 5150 · DRAWING NO. 03-004-5451 · REV B
		SCALE — · CODE IDENT. NO. 50621 · SHEET 1 OF 1

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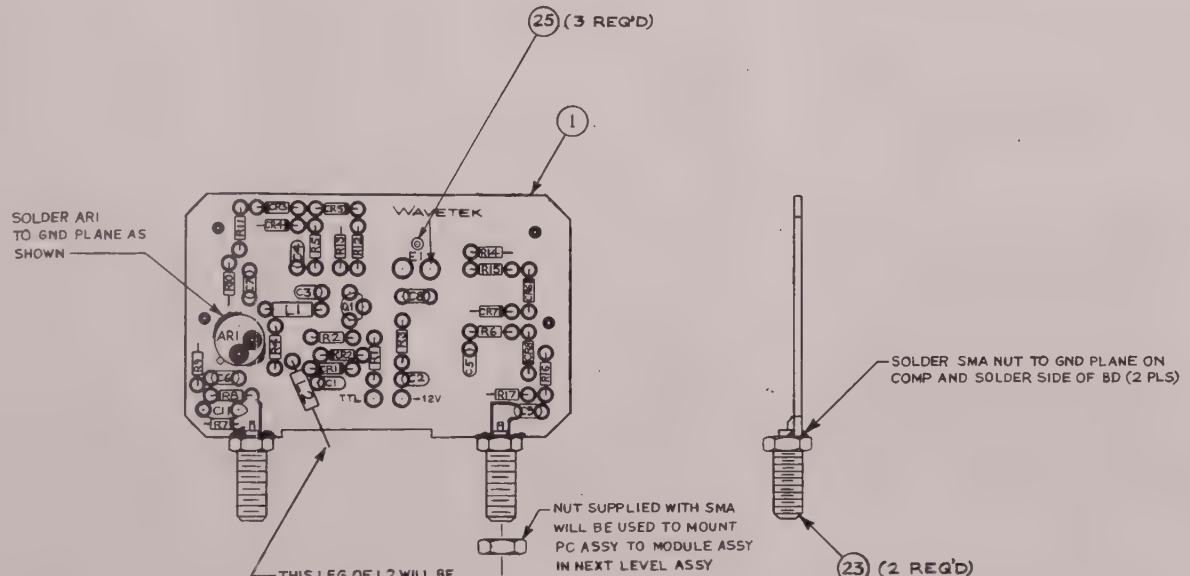
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE			11/1/83
	B	ECO# 1106			3/6/89


25 (3 REQ'D)
1
SOLDER ARI TO GND PLANE AS SHOWN
WAVETEK
ARI
L1
L2
TTL
+12V
THIS LEG OF L2 WILL BE SOLDERED ON MODULE ASSY LEVEL
NUT SUPPLIED WITH SMA WILL BE USED TO MOUNT PC ASSY TO MODULE ASSY IN NEXT LEVEL ASSY (INSTALL AS SHOWN 2 PLS)
SOLDER SMA NUT TO GND PLANE ON COMP AND SOLDER SIDE OF BD (2 PLS)
23 (2 REQ'D)

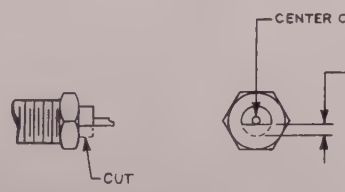


FIG 1

SHEET 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES		
x/x ± 1/64 | .xxx ± .005 | .xx ± .01 | ∠ ± 1°	DRAWN R. Peters	DATE 10/5/83	WAVETEK ROCKLAND Wavetek Rockland, Inc.
MATERIAL:	CHKD	11/1/83	TITLE: P.C. ASSY BANDSWITCH 0 & 1
FINISH:	ENG APPR.	11/1/83	
	MFG APPR.	11/1/83	SIZE C | MODEL NO. 5150 | DRAWING NO. 02-004-5451 | REV B
	ISSUED		SCALE: 2:1 | CODE IDENT 50621 | SHEET 1 OF 2

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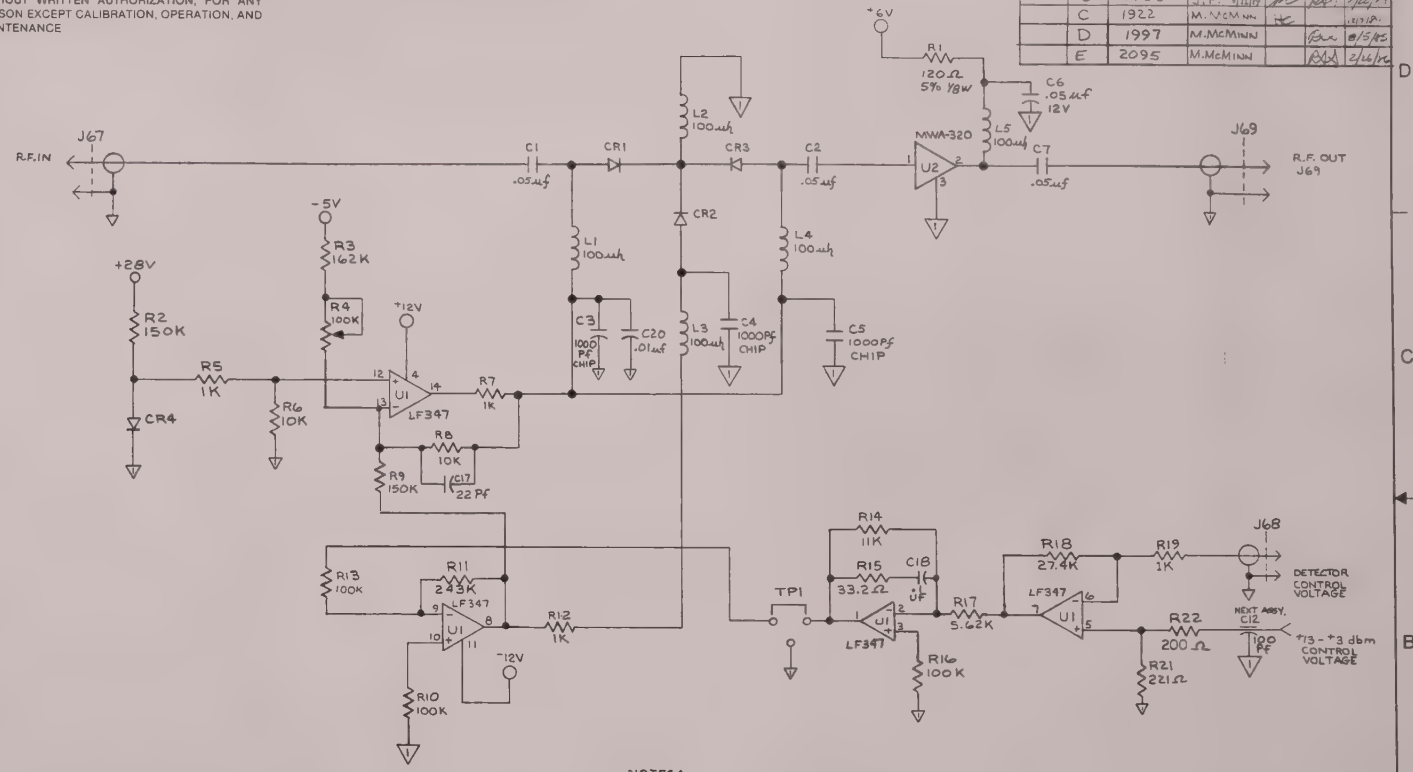
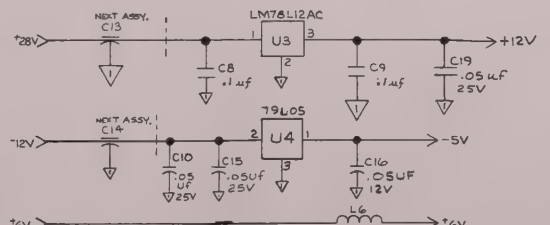
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	1706	J.P.		
	C	1922	M. McMINN		
	D	1997	M.McMINN		
	E	2095	M.McMINN		





NOTES:
1. ALL CR's ARE HP 5082-3080 (PIN)
2. ALL R's ARE 1% 1/8W, (EXCEPT AS NOTED)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES		
x/x ± 1/64 | .xxx ± .005 | .xx ± .01 | ∠ ±1°	DRAWN JP	DATE 11-28-83	TITLE SCHEMATIC V.C.A.
MATERIAL	CHKD		
	ENG APPR.	1/13/84	
FINISH	MFG APPR	1/13/84	
	ISSUED		

WAVETEK

SIZE	MODEL NO.	DRAWING NO	REV
C	5150	03-004-5459	E

SCALE: NONE | CODE IDENT 23338 | SHEET 1 OF 1

R.S. KNAPP

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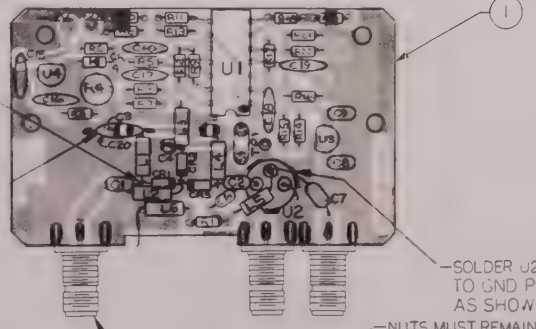
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	1706	JF		
	C	922			
	D	[illegible]			
	E	997			
	F	2045			
	G	2235			



WHERE LEADS ARE SHOWN CROSSED SOLDER POINT TO POINT OFF THE P.C. KEEP LEADS AS SHORT AS POSSIBLE WRAP TIGHTLY & SOLDER

SEE DETAIL "A"

SOLDER U2 3PLS. TO GND PLANE AS SHOWN

NUTS MUST REMAIN WITH ASSEMBLY

(3) 3 REQ'D

DETAIL A
NO SCALE

DR	JF	DATE
CHKD		
ENG		
MFG		
ISSUED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

.XX ±.1mm	.XXX ±.005	±1°	±.5°

MAT PAGE 2&3 "A" SIZE

FIN

WAVETEK

P.C. ASSEMBLY
V.C.A.

SIZE	MODEL NO	DRAWING NO	DEV
C	5150	02-004-5459	G
SCALE 2:1		CODE IDENT 50221	

WAVETEK SD INC. DWG NO. 02 004 5451 REV B

PC ASSY: BANDSWITCH 0/1

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: BANDSWITCH 01/03, 5150	320.5451	1.00
3	AR1	U: WIDE BAND HYB AMP DC-1GHZ	120.7320	1.00
5	R1,R2,R3	R: FX CFLM 1.0K OHM 5% 1/8W	116.2100	3.00
6	R4	R: FX CFLM 100 OHM 5% 1/8W	116.1100	1.00
7	R5,R6,R10,13,R14,R17	R: FX CFLM 270 OHM 5% 1/8W	116.1270	6.00
8	R11,R12,R15,R16	R: FX CFLM 15 OHM 5% 1/8W	116.0150	4.00
9	R8	R: FX CFLM 47 OHM 5% 1/8W	116.0470	1.00
11	R7,R9	R: FX CFLM 130 OHM 5% 1/8W	116.1130	2.00
13	C1-C9	C: FX CER .05UF +20-80 Y5F 12V	100.3502	9.00
15	C11	C: FX CER 10PF 5% NPO 500V	100.0109	1.00
17	CR1-CR5	CR: PIN	133.3542	5.00
18	CR6-CR8	CR: PIN (5082-3080)	133.3080	3.00
19	L1,L2	L: FXD 100 UHY +/-10% MINI.	150.1101	2.00
21	Q1	Q: SIL PNP (2N4122)	136.4122	1.00
23	J51,J52	CONN: SMA BULK RECPT .5"	351.0023	2.00
25	XE1	SOCKET: JMPR (USE W/352.0202)	353.0104	3.00

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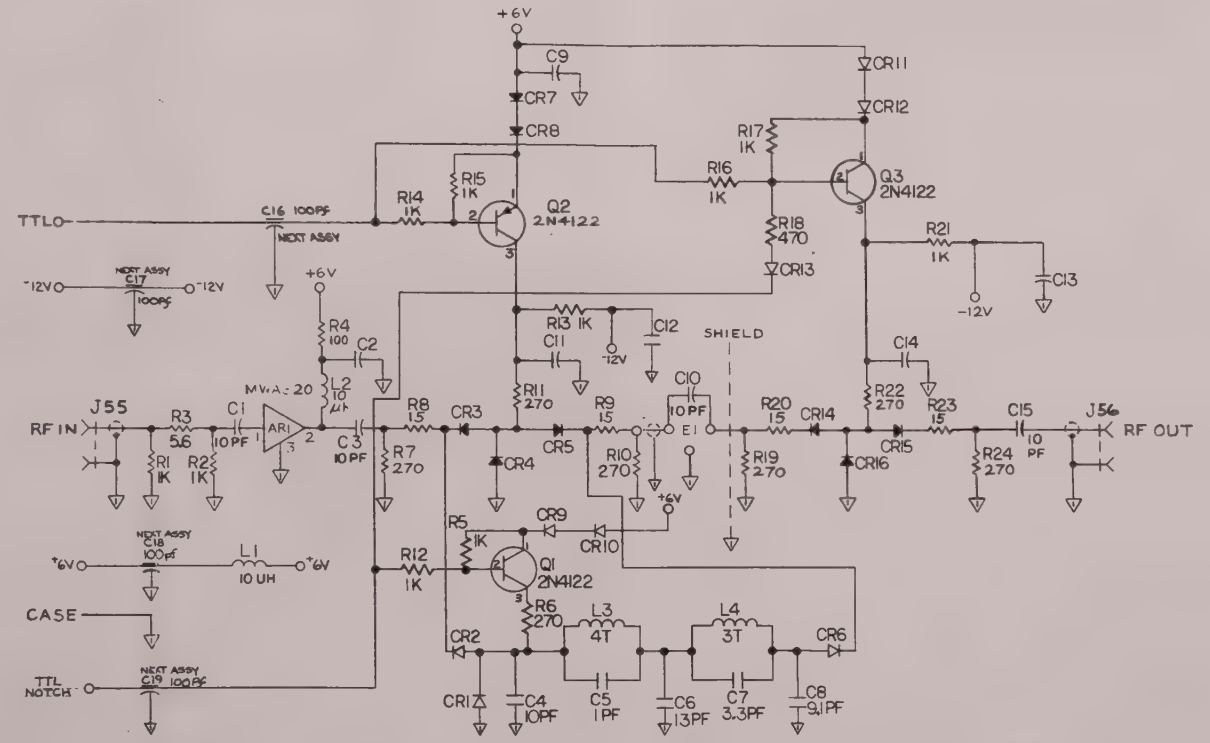
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	PROTO			1-6-84
	B	ECO# 1106			8/27/84



NOTE:
1. UNLESS OTERWISE SPECIFIED.
   a) ALL RESISTORS ARE IN OHMS ±5%, 1/8W.
   b) ALL CAPACITORS ARE .05µf (EXCEPT AS NOTED)
   c) DIODES CR1, CR2, CR6 THRU CR16 ARE KSW3542
      CR3, CR4, CR5 ARE 5082-3080

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
x/x ±1/64 | .xxx ±.005 | .xx ±.01 | ±1°
MATERIAL:
FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN	M. McMinn	11/22/83
CHKD		1/6/84
ENG APPR.		1-6-84
MFG APPR.		1-6-84
ISSUED		

WAVETEK ROCKLAND Wavetek Rockland, Inc.

TITLE: ELECTRICAL SCHEMATIC BANDSWITCH 2

SIZE	MODEL NO.	DRAWING NO.	REV.
C	5150	03-004-5452	B

SCALE: — CODE IDENT 50621 SHEET 1 OF 1

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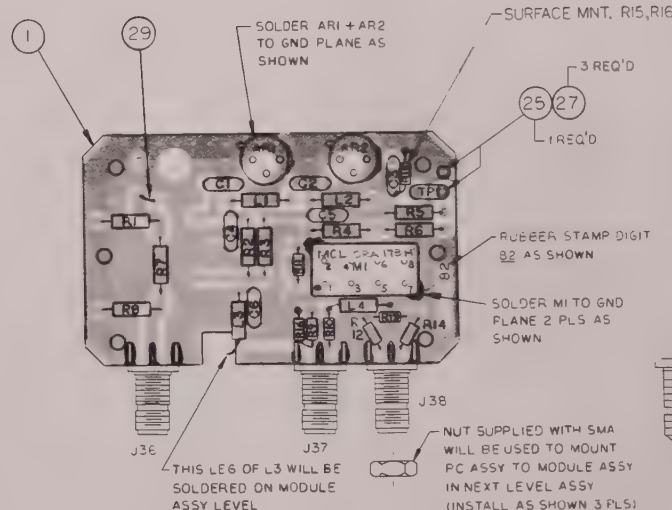
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B				
	C				
	D	ECO 1016	S K		
	E	2238	M McMINN		
	F				
	G				



DR M McMinn	DATE 5/12/83	WAVETEK SAN DIEGO, CALIFORNIA
CHKD		PC ASSY OUTPUT MIXER
ENG		
MFG		
ISSUED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: XX ±.02, XXX ±.005, FRACTIONS ±1/64, ANGLES ±1°

MAT —— FIN ——

SIZE	MODEL NO	DRAWING NO	REV
C	5155	02-004-5482	G

SCALE 2:1 CODE IDENT — SHEET 1 OF 1

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REV	ECO	BY	DATE	APP

EFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/F
C4 C5 C6	CAP, MOND, 01UF +80 -20% 50V	SR215E103ZAT	AVX	100 3105	3
C1 C2 C3	CAP, CER, 3 0PF 25PF 500V NPO	801-036-NPO-509C	TUSON	100 9509	3
R10	RES, CF 39 5% 1/8W	WVTK		110 0390	1
R11 R9	RES, MFLM 150 OHM 1% 1/3W	5063JD150ROF	MEPCO	110 1503	2
R12	RES, CFLM 12 OHM 5% 1/8W			116 0120	1
R3	RES, CFLM 16 OHM 5% 1/4W			116 0161	1
R7	RES, CFLM 18 OHM 5% 1/4W			116 0181	1
[illegible]	RES, CFLM 120 OHM 5% 1/4W			116 1121	1
R1 R8	RES, CFLM 300 OHM 5% 1/4W			116 1301	2
R13 R14	RES, CFLM 430 OHM 5% 1/8W			116 1430	2
R4 R5	RES, CFLM 910 OHM 5% 1/4W			116 1911	2
R6	RES, CFLM 5 6 OHM 5%			116 9561	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO	REV
	KIT, PREWAVE LOAD, 5155A-5482	1208-00-1913	A
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	1/4W				
NONE	PC BD, PREPPED, 5155A-5482	5155A-1914	WVTK	1208-00-1914	1
L1 L2	L, FXD 36 UHY +/-10% MINI	1025-14	DELVN	130 8561	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO	REV
	KIT, PREWAVE LOAD, 5155A-5482	1208-00-1913	A
		PAGE 2	

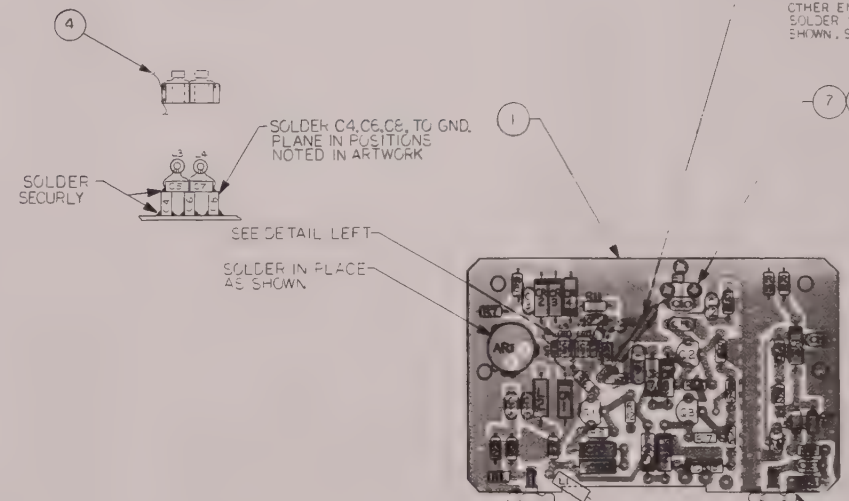
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R15 R16	RES, CFLM 51 OHM 5% 1/8W			116 0510	2
AR1	U: WIDE BAND HYB AMP DC-1 5OHZ			120 7420	1
AR2	U, WIDE BAND HYB AMP DC-1 5OHZ			120 7430	1
NONE	KIT, PREWAVE LOAD, 5155A-5482	5155A-1913	WVTK	1208-00-1913	1
M1	U, DBL BAL MIXER (SRA173M)			[illegible] 500M	1
L4	L, FXD 12 UHY +/-10% MINI	1025-96	DELVN	130 8120	1
L3	L, FXD 56 UHY +/-10% MINI	1025-14	DELVN	130 8561	1
J36 J37 J38	CONN, SMA, PC END LAUNCH JACK, 50 OHM	142-0701	EFJON	331 0032	3
TP1	CONN, PLUG SHORTING (LOW PROF)	4612872-01-03-10	CTC	332 0202	1
27	SOCKET JUMPER	450-3704-01-03-00	CAMBN	353 0103	3
29	WIRE BUSS HD DWN TND #20 AWG	W2020	WEICO	378 0300	25

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO	REV
	PCB ASSY OUT MIXER 0 1-500MHZ	004 5482	G
		PAGE 1	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK San Diego, California
MATERIAL	CHECKED		TITLE
	PROJ. ENGR.		PARTS LIST OUTPUT MIXER
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ± ° ±		SIZE D FSCM NO 23338 DWG NO 004 5482 REV G SCALE MODEL 5155A SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	ECO 1706	JP		


4
SOLDER C4,C6,C8, TO GND. PLANE IN POSITIONS NOTED IN ARTWORK
SOLDER SECURLY
SEE DETAIL LEFT
SOLDER IN PLACE AS SHOWN
1
3
SOLDER ONE END OF CABLE TO PAD SUPPLIED AT R9-R10 JUNCTION, THE OTHER END TO THE BASE OF C10. SOLDER SHIELD TO GROUND AS SHOWN. SEE BELOW FOR STRIP DETAILS.
7
9
.90
.15
.15
.05 Ø
STRIP DETAILS
6
.55
NUTS MUST REMAIN WITH ASSEMBLY (DO NOT TIGHTEN)
SOLDER EACH SMA SPLS. CENTER CONTACT TO LAND. EACH SIDE OF HEX TO GND. PLANE ON COMP. & SOLDER SIDE. (USE FIXTURE TO MOUNT SMA'S)

"SMA" ALTERATION

CUT RIGHT ANGLE NOTCH OUT OF TEFLON WITH EXACTO KNIFE AS SHOWN. PLACE SMA ON P.C. WITH THE NOTCH DOWN ON THE P.C., SOLDER IN PLACE AS SHOWN ABOVE. CAUTION - SMA'S MUST BE CENTERED ON P.C. LANDS. (USE FIXTURE TO MOUNT SMA'S)

DR	DATE 7-1-74
CHKD	
ENG	
MFG	
ISSUED	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

XX ± .01	XXX ± .005	ANGLES ± 1°

MAT SEE SHEET 2 "A" SIZE

FIN

WAVETEK ROCKLAND Wavetek Rockland, Inc.

PRINTED WIRING BOARD
P.C. ASSEMBLY BANDSWITCH NO. 2

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5452	B

SCALE 2:1 CODE IDENT 50221 SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5452 REV B

PC ASSY: BANDSWITCH 2

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: BANDSWITCH 02, 5150	320.5452	1.00
3	AR1	U: WIDE BAND HYB AMP DC-1GHZ	120.7320	1.00
4	6"	WIRE: BUSS TINNED #22GA	378.0601	1.00
5	Q1,Q2,Q3	Q: SIL PNP (2N4122)	136.4122	3.00
6	J55,J56	CONN: SMA BULK RECPT .5"	351.0023	2.00
7	XE1	SOCKET: JUMPER	353.0103	3.00
8	.90"	CABLE: COAX RIGID UT-47 50 OHM	378.4612	1.00
9	E1	PLUG: SHORTING (LOW PROF)	352.0202	1.00
10	R3	R: FX CFLM 5.6 OHM 5% 1/8W	116.9560	1.00
11	R8,R9,R23,R20	R: FX CFLM 15 OHM 5% 1/8W	116.0150	4.00
13	R4	R: FX CFLM 100 OHM 5% 1/8W	116.1100	1.00
15	R7,R6,R10,R11,R19,R22,R24	R: FX CFLM 270 OHM 5% 1/8W	116.1270	7.00
17	R18	R: FX CFLM 470 OHM 5% 1/8W	116.1470	1.00
19	R1,2,5,12,13,14,15,16,17,21	R: FX CFLM 1.0K OHM 5% 1/8W	116.2100	10.00
21	C2,C9,C11,C12,C13,C14	C: FX CER .05UF +20-80 Y5F 12V	100.3502	6.00
23	C1,C3,C10,C15	C: FX CER 10PF 5% NPO 500V	100.0109	4.00
24	C5	C: FX CER CHIP 1.0PF	107.9102	1.00
25	C8	C: FX CER CHIP 9.1PF	107.9912	1.00
26	C4	C: FX CER CHIP 10PF	107.0102	1.00
27	C6	C: FX CER CHIP 13PF	107.0132	1.00
28	C7	C: FX CER CHIP 3.3PF	107.9332	1.00
30	L1,L2	L: FXD 10.0 UHY +/-10% MINI.	150.0101	2.00
31	L4	L: TOROID, 3 TURN, (T7/36AWG)	012.1060	1.00
32	L3	L: TOROID, 4 TURN, (T7/36AWG)	012.1061	1.00
33	CR1,CR2,CR6 THRU CR16	CR: PIN	133.3542	13.00
34	CR3,CR4,CR5	CR: PIN (5082-3080)	133.3080	3.00

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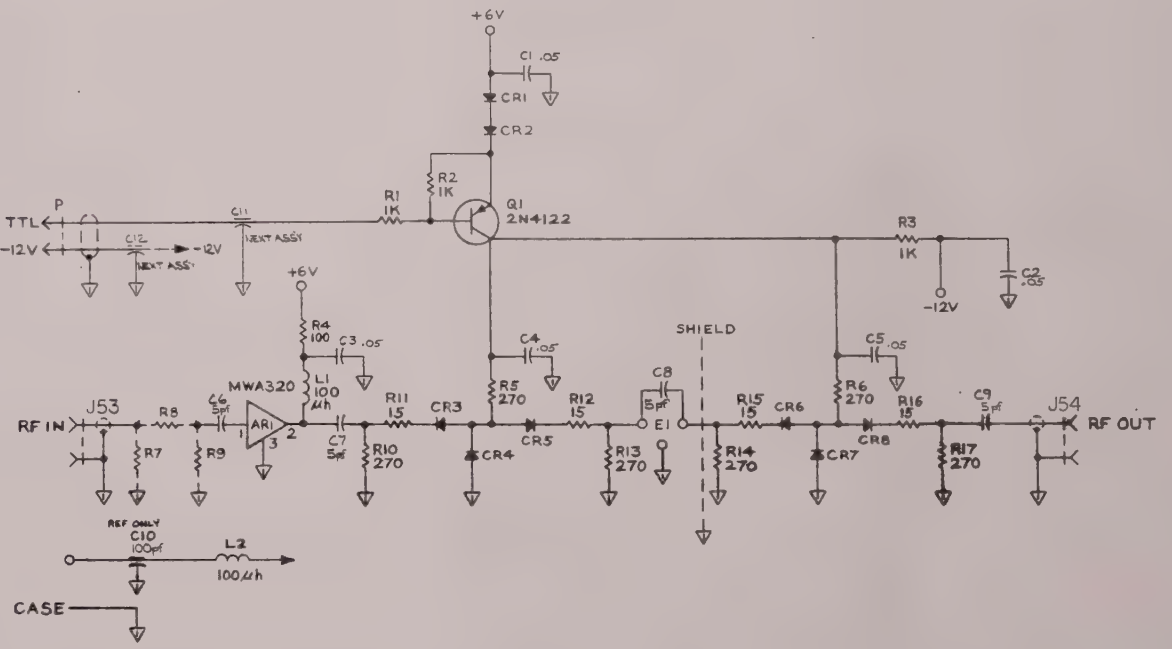
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A				
	B	RELEASE			
	C	REDRAWN			7/19/84
	D	2091	M. McMINN		7/16/86



NOTE:
1. UNLESS OTERWISE SPECIFIED.
   a) ALL RESISTORS ARE IN OHMS ±5%, 1/8W.
   b) ALL CAPACITORS ARE µf UNLESS OTHERWISE NOTED
   c) DIODES CR1-CR5 ARE KSW3542
      CR6-CR8 ARE 5082-3080

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND — Wavetek Rockland, Inc.
x/x ±1/64 .xxx ±.005 .xx ±.01 ∠ ±1°	DRAWN JP 11-17-83	TITLE: ELECTRICAL SCHEMATIC BANDSWITCH 3
MATERIAL:	CHKD 1/6/84	
	ENG APPR 1-6-84	
FINISH:	MFG APPR 1-6-84	SIZE C · MODEL NO 5150 · DRAWING NO 03-004-5453 · REV D
	ISSUED	SCALE: NONE · CODE IDENT 50621 · SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY IN-
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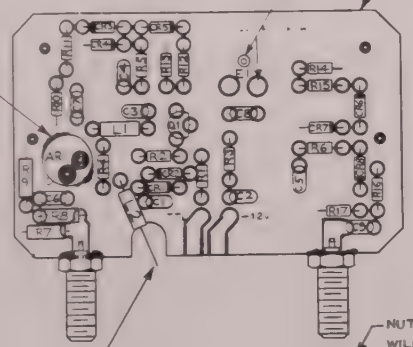
WAVETEK AND MAY NOT BE REPRODUCED
WITHOUT WRITTEN AUTHORIZATION FOR ANY
REASON EXCEPT CALIBRATION AND FIELD
MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			11/1/80
	B	RELEASE			
	C	REDRAWN PER ECO			7/5/84
	D	2091	M. McMINN		2/2/86

(25) (3 REQ'D)

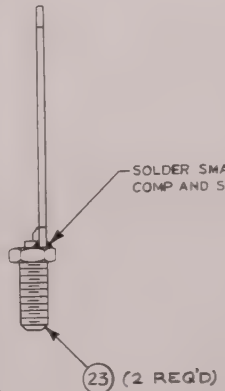
(1)

SOLDER AR1 TO GND PLANE AS SHOWN



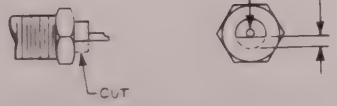
THIS LEG OF L2 WILL BE SOLDERED ON MODULE ASSY LEVEL

NUT SUPPLIED WITH SMA WILL BE USED TO MOUNT PC ASSY TO MODULE ASSY IN NEXT LEVEL ASSY (INSTALL AS SHOWN 2 PLS)



SOLDER SMA NUT TO GND PLANE ON COMP AND SOLDER SIDE OF BD (2 PLS)

(23) (2 REQ'D)



CENTER CONDUCTOR (REF)

REMOVE NYLON INSULATOR AS SHOWN KEEPING THE CUT PARALLEL TO FLAT EDGE OF SMA NUT

CUT

FIG 1

SHEET 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

± .164 ± .005 ± .01 ∠ ±°

MATERIAL

FINISH

DRAWN	TM	2/16/84
CHKD		
ENG APPR		7/5/84
MFG APPR		7/5/84
ISSUED		

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: P.C. ASSY BANDSWITCH 3

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5453	D

SCALE 2:1 | CODE IDENT 50621 | SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5453 REV D

PC ASSY: BANDSWITCH 3

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: BANDSWITCH 01/03, 5150	320.5451	1.00
3	AR1	U: WIDE BAND HYB AMP DC-1GHZ	120.7320	1.00
5	R1,R2,R3	R: FX CFLM 1.0K OHM 5% 1/8W	116.2100	3.00
6	R4	R: FX CFLM 100 OHM 5% 1/8W	116.1100	1.00
7	R5,R6,R10,R13,R14,R17	R: FX CFLM 270 OHM 5% 1/8W	116.1270	6.00
8	R11,R12,R15,R16	R: FX CFLM 15 OHM 5% 1/8W	116.0150	4.00
13	C1-C5	C: FX CER .05UF +20-80 Y5F 12V	100.3502	5.00
15	C6-C9	C: FX CER 5.0PF .25PF NPO 500V	100.9509	4.00
17	CR1-CR5	CR: PIN	133.3542	5.00
18	CR6-CR8	CR: PIN (5082-3080)	133.3080	3.00
19	L1,L2	L: FXD 100 UHY +/-10% MINI.	150.1101	2.00
21	Q1	Q: SIL PNP (2N4122)	136.4122	1.00
23	J53,J54	CONN: SMA BULK RECPT .5"	351.0023	2.00
25	XE1	SOCKET: JMPR (USE W/352.0202)	353.0104	3.00
27	R7,R9	R: FX CFLM 1.0K OHM 5% 1/8W	116.2100	2.00
28	R8	R: FX CFLM 4.7 OHM 5% 1/8W	116.9470	1.00

SECTION 21
SUMMER MODULE

21.1 INTRODUCTION

The Summer Module (SM) accepts the bandswitch 0 and 1, 500-750 MHz bandpass filter and 750-1000 bandpass filter signals and routes them into the voltage controlled attenuator circuit. For any given frequency, only one of the three circuits will have a input signal to the summer module.

21.2 THEORY OF OPERATION

Refer to schematic 03-004-5473. The 1 to 500 MHz output from bandswitch 0 and 1 enters the summer module at J63. This signal passes through an attenuator (R9, R10 and R11) to 10 dB amplifier, AR1. The 500 to 750 MHz output from the 500-750 MHz bandpass filter enters the summer module at J64, passing through an attenuator (R12, R13 and R14) to AR2 where it is amplified 9 dB. The 750 to 1000 MHz output from the 750-1000 bandpass filter enters the summer module at J65 and is amplified 9 dB by AR3 after passing through attenuator R12, R13 and R14. The output of these three amplifiers (only one will have a signal) are summed at the junction of R3 and R4, then amplified 6 dB by AR4 before reaching the VCA via output connector J66.

21.3 SPECIFICATIONS

Input Signals	1 to 500 MHz. 500 to 750 MHz. 750 to 1000 MHz.
Output Signal	1 to 1000 MHz.
DC Supply	+6.0V at 150 mA.
Connectors	Four SMA female.

21.4 MAINTENANCE

21.4.1 Preventive Maintenance

Preventive maintenance is not required for the summer module. Normal operation is indicated by the presence of correct outputs.

21.4.2 Alignment/Calibration

No alignment or calibration is necessary after replacement of individual parts.

21.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If the summer module has been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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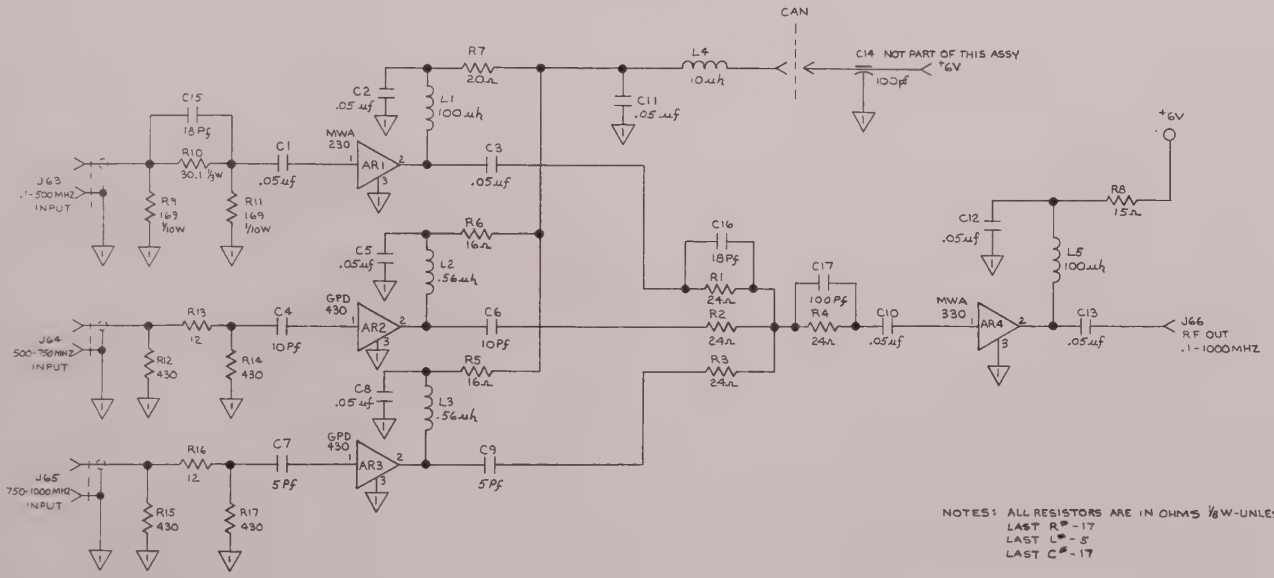
	A	RELEASE			1-6-84
	B	ECO# 1706			7/9/84



NOTES: ALL RESISTORS ARE IN OHMS 1/8W-UNLESS NOTED
LAST R# - 17
LAST L# - 5
LAST C# - 17

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
x/x ± 1/64 | .xxx ± .005 | .xx ± .01 | ∠ ± 1°
MATERIAL:
FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN	JP	11-17-83
CHKD		1/6/84
ENG APPR		1-6-84
MFG APPR		1/6/84
ISSUED		

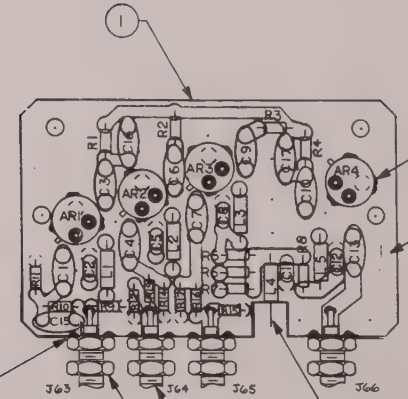
WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: SCHEMATIC SUMMER

SIZE	MODEL NO.	DRAWING NO.	REV.
C	5150	03-004-5473	B

SCALE: NONE | CODE IDENT 50621 | SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			1-6-84
	B	706	JP		7/9/84



SOLDER ARI THRU AR4 TO GROUND PLANE IN 3PLS (TYP. AS SHOWN)

STAMP CURRENT REV. LETTER

SOLDER SMA'S TO P.C. IN 4 PLS. NUT TO GND PLANE ON SOLDER SIDE, NUT TO GND PLANE EACH SIDE OF CENTER LAND, AND TO CENTER LAND

THIS END OF L4 TO BE TERMINATED LATER

NUTS MUST REMAIN WITH ASSEMBLY

"SMA" ALTERATION

CUT NOTCH OUT OF TEFLON WITH EXACTO AS SHOWN, NOTCH ORIENTED DOWN ON COMP SIDE OF P.C.

DR	JP	DATE
CHKD		1/6/84
ENG		1-6-84
MFG		1-6-84
ISSUED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:

MAT SHEET 2 "A" SIZE

FIN

WAVETEK ROCKLAND Wavetek Rockland, Inc.

P.C. ASSEMBLY SUMMER

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5473	B

SCALE 2:1 CODE IDENT 50621 SHEET 1 OF 2

WAVETEK SD INC. DWG NO. 02 004 5473 REV B

PC ASSY: SUMMING MODULE

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: SUMMING MODULE, 5150	320.5473	1.00
3	-	CONN: SMA BULK RECPT .5"	351.0023	4.00
5	AR1	U: WIDE BAND HYB AMP DC-600MHZ	120.7230	1.00
7	AR2,AR3,AR4	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7430	3.00
8	R13,R16	R: FX CFLM 12 OHM 5% 1/8W	116.0120	2.00
9	R8	R: FX CFLM 15 OHM 5% 1/8W	116.0150	1.00
10	R10	R: FX MFLM 30.1 OHM 1% 1/3W	119.3015	1.00
11	R5,R6	R: FX CFLM 16 OHM 5% 1/8W	116.0160	2.00
12	R9,R11	R: FX MFLM 169 OHM 1% 1/10W T2	110.1691	2.00
13	R7	R: FX CFLM 20 OHM 5% 1/8W	116.0200	1.00
14	R12,R14,R15,R17	R: FX CFLM 430 OHM 5% 1/8W	116.1430	4.00
15	R1 THRU R4	R: FX CFLM 24 OHM 5% 1/8W	116.0240	4.00
17	C15,16	C: FX CER 18PF 5% NPO 500V	100.0189	2.00
18	C17	C: FX CER 100PF 10% X5F 500V	100.1105	1.00
19	C13	C: FX CER .05UF +20-80 Y5F 12V	100.3502	0.00
19	C1,C2,C3,C5,C8,C10,C11,C12,	C: FX CER .05UF +20-80 Y5F 12V	100.3502	9.00
21	C7,C9	C: FX CER 5.0PF .25PF NPO 500V	100.9509	2.00
23	C4,C6	C: FX CER 10PF 5% NPO 500V	100.0109	2.00
25	L2,L3	L: FXD .56 UHY +/-10% MINI.	150.8561	2.00
27	L4	L: FXD 10.0 UHY +/-10% MINI.	150.0101	1.00
29	L1,L5	L: FXD 100 UHY +/-10% MINI.	150.1101	2.00

SECTION 22
ATTENUATOR/OUTPUT CIRCUITS

22.1 INTRODUCTION

The Voltage Controlled Attenuator (VCA) circuit, controlled by the front panel, sets the output amplitude by attenuating the RF signal before it reaches the Output Amplifier (OA). The output amplifier provides the final (fixed) RF signal gain prior to its being sent to the output connector.

22.2 THEORY OF OPERATION

22.2.1 Voltage Controlled Attenuator

Refer to schematic 03-004-5459. The RF signal from the summer module enters the VCA at J67. As the voltages at the anodes of CR1, CR2 and CR3 increase, their resistance to the RF signal also increases. Because CR1 and CR3 are in series with the RF signal, an increase in resistance of these diodes decreases the RF signal level at U2 pin 1. With CR2 in parallel with the RF signal, a decrease in resistance of this diode decreases the RF signal level at U2 pin 1 by shunting it to ground through C4.

The amount of attenuation provided by the VCA is directly proportional to the control voltage at C12. As the control voltage increases, the voltage at U1 pin 9 decreases, increasing the voltage at pin 8. This forward biases CR2, providing a parallel path through C4 for the RF signal. U1 pin 8 also provides an input at U1 pin 13. As the voltage at U1 pin 8 increases, the voltage at U1 pin 14 decreases, placing a more negative voltage at the anodes of both CR1 and CR3, increasing their resistance to the RF signal.

Feedback to the VCA from the output amplifier is provided at J68. This feedback maintains the output amplifier signal at a constant level as determined by the VCA. Temperature compensation is provided by diode CR4 at U1 pin 12. U2 provides final amplification of the RF signal before it reaches J69, the RF output.

For the Model 5156A, the control voltage originates from P4 pin 30 on the BCD amplifier board 002.5417. For the Model 5155A, it originates from J4 pin 6 on the front panel board 002.5423.

22.2.2 Output Amplifier

Refer to schematic 03-004-5460. The RF signal from the voltage controlled attenuator enters the Output Amplifier (OA) at J70. This signal passes through an attenuator (R11, R12 and R13) to a string of four amplifiers (AR1, AR2, AR3 and AR4) with a total gain of 20 dB. As the amplitude between AR3 and AR4 increases, the output detector control voltage at J71 decreases. This 5voltage provides feedback to the VCA to maintain the output amplifier signal at the desired level as determined by the VCA control voltage.

22.3 SPECIFICATIONS

22.3.1 Voltage Controlled Attenuator

Input Signals	1 to 1000 MHz. DC control voltage.
Output Signal	1 to 1000 MHz.
Bandwidth	DC to 1500 MHz.
DC Supply	+6.0V at 25 mA. −12.4V at 10 mA. +28V at 18 mA.
Connectors	Three SMA female.

22.3.2 Output Amplifier

Overall Gain	+20 dBm.
Input Signal	1 to 1000 MHz.
Output Signal	1 to 1000 MHz. DC control voltage proportional to signal amplitude.
DC Supply	+6.0V at 200 mA.
Connectors	Three SMA female.

22.4 MAINTENANCE

22.4.1 Preventive Maintenance

Preventive maintenance is not required for the VCA or output amplifier modules. Normal operation is indicated by the presence of correct outputs.

22.4.2 Alignment/Calibration

Field or customer alignment of these modules is not advised. If realignment is required, return both assemblies to the factory for service.

22.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If either the VCA or output amplifier modules have been isolated as the source of the problem, field replacement of the faulty assembly may restore partial operation of the unit. However, the initial checkout procedure located in section 2 of this manual should be performed to verify complete operation.

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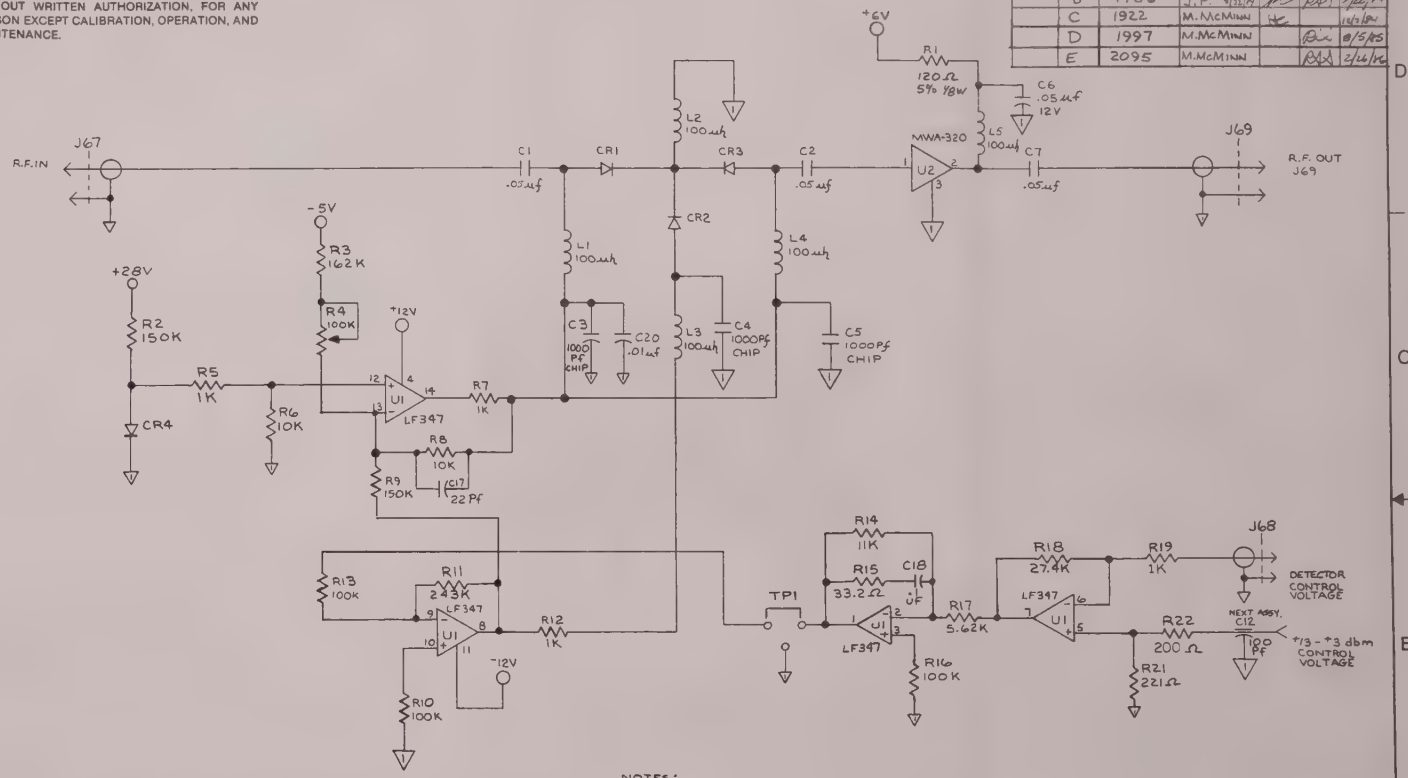
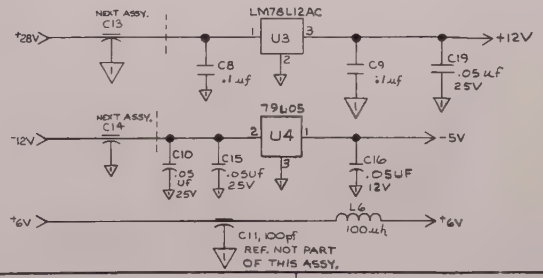
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE			
	B	1706	J.P.		8/22/84
	C	1922	M. McMINN		1/13/84
	D	1997	M. McMINN		8/5/85
	E	2095	M. McMINN		2/6/86





NOTES:
1. ALL CR's ARE HP 5082-3080 (PIN)
2. ALL R's ARE 1% 1/3W, (EXCEPT AS NOTED)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
x/x ± 1/64 | .xxx ± .005 | .xx ± .01 | ∠ ± 1°
MATERIAL:
FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN	JP	1-28-83
CHKD		
ENG APPR.		1/13/84
MFG APPR.		1/13/84
ISSUED		

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

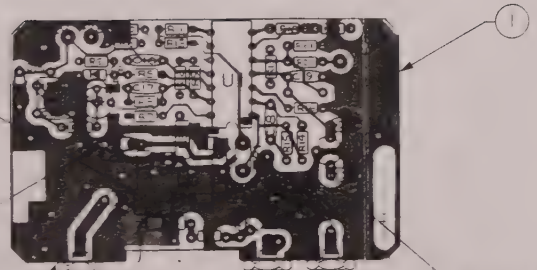
TITLE: SCHEMATIC V.C.A.

SIZE	MODEL NO.	DRAWING NO.	REV
C	5150	03-004-5459	E

SCALE: NONE | CODE IDENT 23338 | SHEET 1 OF 1

R.S. KNAPP

ZONE	LTR	ECO NO.	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	706	JF		
	C	[illegible]			
	D	697			
	E	2695			


1
U
SEE DETAIL A
WHERE LEADS ARE SHOWN CROSSED SOLDER BRIDGE AT POINT OF THE P.C. KEEP LEADS AS SHORT AS POSSIBLE WHERE "NO-C" IS SOLDER

SOLDER J2 3 PLS. TO GND PLANE AS SHOWN

NUTS MUST REMAIN WITH ASSEMBLY

(3) 3 REQ'D

WHERE POSSIBLE SOLDER SMA'S 4 PLS. CENTER CONTACT TO LAND, EACH SIDE OF HEX TO GND PLANE ON COMP. SIDE & ALONG ENTIRE HEX ON SOLDER SIDE TO GND.

SMA ALTERATION

CUT RIGHT ANGLE NOTCH OUT OF TEFLON WITH EXACTO KNIFE AS SHOWN. PLACE SMA ON P.C. WITH THE NOTCH DOWN ON COMP SIDE. NOTE: SMA'S MUST BE CENTERED ON P.C. LANDS. USE FIXTURE TO MOUNT SMA'S.

DETAIL A
NO SCALE

DR	DATE	WAVETEK ROCKLAND Wavetek Rockland, Inc
CHKD		
ENG		P.C. ASSEMBLY V.C.A
MFG		
ISSUED		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE		
MATERIAL [illegible] SIZE	SIZE C	MODEL NO 5150
FIN	SCALE 2:1	DRAWING NO 04-5459 F
	CODE IDENT [illegible]	SHEET OF 2

WAVETEK SD INC. DWG NO. 02 004 5459 REV F

PC ASSY: VC-ATTENUATOR

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: VC-ATTENUATOR MODULE, 515	[illegible]	1.00
3	-	CONN: SMA BULK RECPT .5"	351.0023	3.00
5	U2	U: WIDE BAND HYB AMP DC-1GHZ	120.7320	1.00
6	U1	U: QD LIN BIFET OP-AMP (LF347)	120.2047	1.00
8	U3	Q: P.V. REG 12V TO-92 (78L12C)	120.0122	1.00
9	U4	Q: N.V. REG 5V (79L05)	[illegible]	1.00
11	CR1,CR2,CR3,CR4	CR: PIN (5082-3080)	133.3080	4.00
13	L1,L2,L3,L4,L5,L6	L: FXD 100 UHY +/-10% MINI.	150.1101	[illegible]
15	C1,C2,C6,C7,C16	C: FX CER .05UF +20-80 Y5F 12V	100.3502	5.00
16	C3,C4,C5	C: FX CER CHIP 1000PF	107.2102	[illegible]
17	C8,C9	C: FX MONO 0.1UF Z5U 50V	100.4102	[illegible]
18	C10,C15,C19	C: FX CER .05UF 20% YSP 25V	[illegible]	[illegible]
19	C17	C: FX CER 22PF 5% NPO 500V	[illegible]	1.00
20	C18	C: FX CER .1UF +80 -20% 12V	[illegible]	1.00
21	C20	C: FX CER .01UF +80 -20% 100V	[illegible]	1.00
22	R1	R: FX CFLM 120 OHM 5% 1/8W	116.1120	1.00
23	R2,R9	R: FX MFLM 150.0K OHM 1% 1/3W	113.1505	2.00
24	R3	R: FX MFLM 162.0K OHM 1% 1/3W	113.1625	1.00
25	R4	R: VAR CMT 100K 1/4" RND	118.4101	1.00
26	R5,R7,R12,R19,R22	R: FX MFLM, 1.00K 1% 1/3W T0	111.1005	5.00
27	R6,R8	R: FX MFLM 10.0K OHM 1% 1/3W	112.1005	2.00
28	R10,R13,R16	R: FX MFLM 100.0K OHM 1% 1/3W	113.1005	[illegible]
29	R11	R: FX MFLM 243.0K OHM 1% 1/3W	113.2435	1.00
30	R14	R: FX MFLM 11.0K OHM 1% 1/3W	112.1105	1.00
31	R15	R: FX MFLM 33.2 OHM 1% 1/3W	119.3325	[illegible]
32	R17	R: FX MFLM 5.62K OHM 1% 1/3W	111.5625	1.00
33	R18	R: FX MFLM 27.4K OHM 1% 1/3W	112.2745	1.00
35	R21	R: FX MFLM 221 OHM 1% 1/3W	110.2215	1.00
37	-	SOCKET: JUMPER	353.0103	3.00
39	-	PLUG: SHORTING (LOW PROF)	352.0202	1.00

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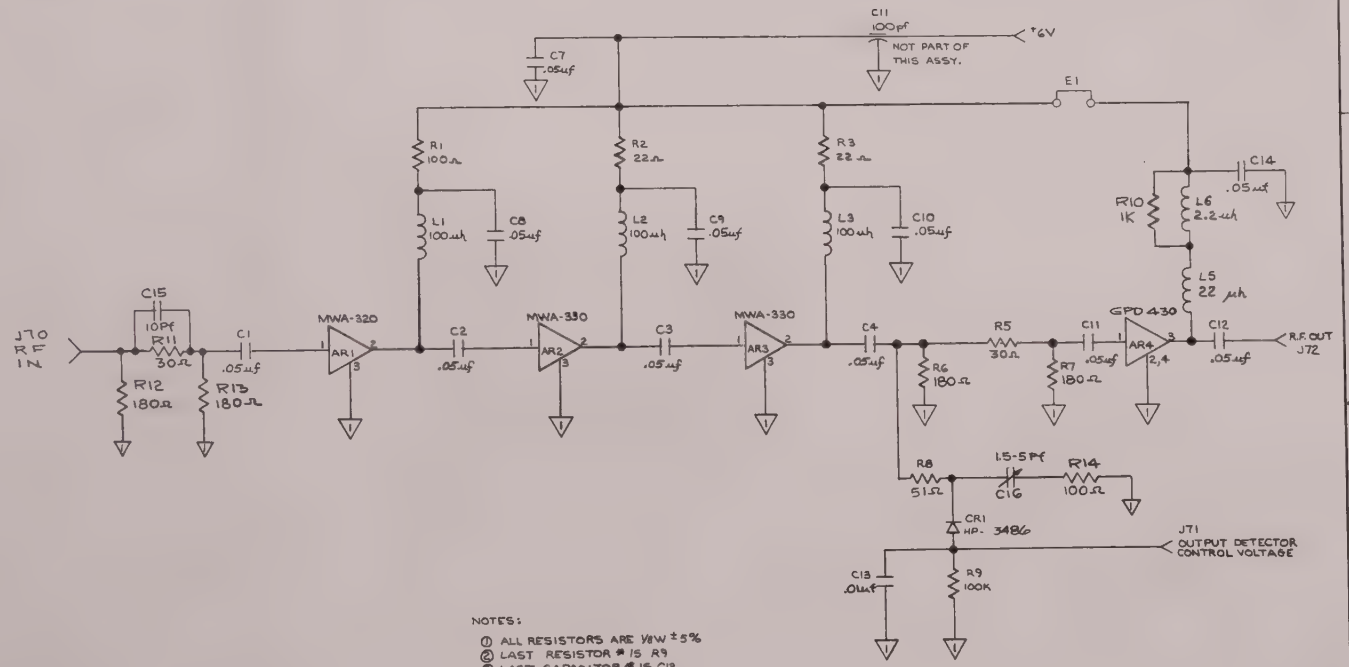
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	B	RELEASE		RAS	1/27/84
	C	ECO# 1706			3/1/85
	D	2018	M. McMINN	RAS	9/24/85
	E	2111	M. McMINN	RAS	4/2/86



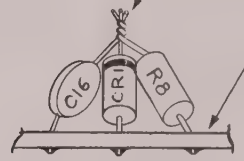
NOTES:
1. ALL RESISTORS ARE ¼W ±5%
2. LAST RESISTOR # IS R9
3. LAST CAPACITOR # IS C13

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND	Wavetek Rockland, Inc.
x/x ±1/64 .xxx ±.005 .xx ±.01 ∠ ±1°	DRAWN JP 12-12-83	TITLE	SCHEMATIC OUTPUT AMPLIFIER
MATERIAL: //	CHKD 1/27/84		
FINISH: //	ENG APPR. RAS 1/27/84	SIZE C	MODEL NO. 5150
	MFG APPR. 1/27/84	DRAWING NO	03-004-5460 REV E
	ISSUED	SCALE: NONE	CODE IDENT 50621 SHEET 1 OF 1

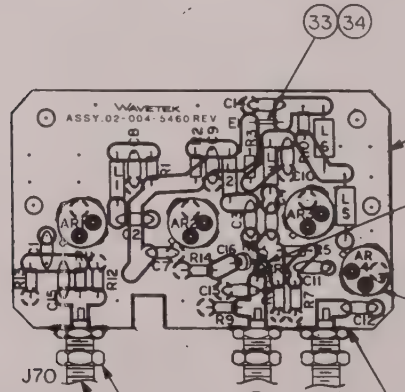
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	B	RELEASE		[illegible]	1/27/84
	C	1706	JP		3/5/85
	D	1981	M. McMINN		6/12/86
	E	2018	B. SIMMS		9/26/85
	F	2111	M. McMINN		4/2/86
	G	2127	[illegible] 4/5/86		6/3/86

TWIST & SOLDER LEADS TOGETHER
(DO NOT ALLOW LEADS TO TOUCH P.W.B.)

(1) (REF)



DETAIL A
(APPROX 4:1)


33
34
1
WAVETEK
ASSY.02-004-5460 REV
SEE DETAIL "A"
SOLDER CASE TO GND PLANE AS SHOWN. TYP 4 PLACES.
J70
J71
J72
NUTS MUST REMAIN WITH ASSY.
3
SOLDER SMA'S 4PLS. CENTER CONTACT TO LAND, EACH SIDE OF HEX TO GND. PLANE ON COMP. SIDE & ALONG ENTIRE HEX ON SOLDER SIDE TO GND. WHEN POSSIBLE.

"SMA" ALTERATION

CUT RIGHT ANGLE NOTCH OUT OF TEFLON WITH EXACTO KNIFE AS SHOWN. PLACE SMA ON P.C. WITH THE NOTCH DOWN ON COMP. SIDE.
NOTE: SMA'S MUST BE CENTERED ON P.C. LANDS, USE FIXTURE TO MOUNT SMA'S

DR	JP	DATE 12-13-83
CHKD	R	1/27/84
ENG	RdS	1/27/84
MFG	RdS	1/27/84
ISSUED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:
.XX ± .01 ANGLES ± 1°
.XXX ± .005 .XXXX ± .001
MAT SHEET 2"A" SIZE
FIN ——

WAVETEK ROCKLAND Wavetek Rockland, Inc.

P.C. ASSEMBLY
OUTPUT AMPLIFIER

SIZE	MODEL NO	DRAWING NO	REV
C	5150	02-004-5460	G
SCALE 2:1	CODE IDENT 50621	SHEET 1 OF 2	

WAVETEK SD INC. DWG NO. 02 004 5460 REV F

PC ASSY: OUTPUT AMP

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: "OA0" MODULE, 5150	320.5460	1.00
3	-	CONN: SMA BULK RECPT .5"	351.0023	3.00
5	AR1	U: WIDE BAND HYB AMP DC-1GHZ	120.7320	1.00
7	AR3,AR2	U: WIDE BAND HYB AMP DC-1GHZ	120.7330	2.00
8	AR4 GPD 430	U: WIDE BAND HYB AMP DC-1.5GHZ	120.7430	1.00
9	R2,R3	R: FX CFLM 22 OHM 5% 1/8W	116.0220	3.00
11	R1,R14	R: FX CFLM 100 OHM 5% 1/8W	116.1100	1.00
13	R8	R: FX CFLM 51 OHM 5% 1/8W	116.0510	1.00
15	R9	R: FX CFLM 100K OHM 5% 1/8W	116.4100	1.00
17	R6,R7,R12,R13	R: FX CFLM 180 OHM 5% 1/8W	116.1180	4.00
19	R10	R: FX CFLM 1.0K OHM 5% 1/4W	116.2101	1.00
21	R5,R11	R: FX CFLM 30 OHM 5% 1/8W	116.0300	2.00
24	C11,C12	C: FX CER .05UF 20% Y5P 25V	100.3501	2.00
25	C1-C4,C7-C10,C14	C: FX CER .05UF +20-80 Y5F 12V	100.3502	9.00
26	C16	C: VAR CER 1.5-5PF 250V	108.0050	1.00
27	CR1 HP-3486	CR: DETECTOR	133.3486	1.00
28	L5	L: FXD 22 UHY +/-20%	150.0222	1.00
29	L1,L2,L3	L: FXD 100 UHY +/-10% MINI.	150.1101	3.00
30	L6	L: FXD 2.2 UHY +/-10% SHLD	150.9220	1.00
31	C13	C: FX CER .01UF +80 -20% 100V	100.3104	1.00
32	C15	C: FX CER 10PF 5% NPO 500V	100.0109	1.00
33	E1 1"	WIRE: BUSS HD DWN TND #20 AWG	378.0500	1.00
34	1"	SLVNG: TEFLON #20AWG	378.5202	1.00

SECTION 23
POWER SUPPLY CIRCUITS

23.1 INTRODUCTION

The power supplies used in this unit generate dc voltages of +5.4, +6, +23, +28 and -12.6V. They are conventional in design, with short-circuit protection and fold-back current limiting. If ever found to be defective, they may be replaced as a unit. For a description of power supply conditions during standby, refer to paragraph 23.2.4.

23.2 THEORY OF OPERATION

23.2.1 Power Supply 1 (HCC512-501)

This power supply generates regulated dc voltages of +5.4V, which powers the TTL and MECL logic, and −12.6V for the transistor amplifiers. An unregulated voltage of +23V is also generated from this board.

Refer to schematic 03-174-5013. The +5.4V power supply is fed by split primary transformer T1. Silicon rectifiers CR1 through CR4 and electrolytic capacitor C1 provide unregulated dc to regulator U1. In conjunction with Q2, this regulator sets the reference and gain. Increased power output is provided by series-pass transistor Q1.

The −12.6V power supply is also fed by transformer T1. Unregulated dc to power U2 comes from rectifiers CR5 through CR8 and capacitor C4. U2 and Q4 set the reference and gain. Increased power output is provided by Q3. Under normal operating conditions, the -12.6V output is fed to the mainboard (see schematic 03-004-5429) and through S1 to L12 where it drops 0.2V to become −12.4V. This voltage is then distributed to several circuits in the unit.

Both the +5.4 and −12.6V supplies are short-circuit proof with fold-back current limiting.

Unregulated +23V, which powers the +5.4V regulator, is tapped and used in other sections of the unit.

Component designators are screened on the printed circuit board to aid in troubleshooting. If desired, the power supply assembly may be replaced as a unit.

23.2.2 Power Supply 2 (MAA-500)

This power supply generates a dc voltage of +28V. Refer to schematic 03-174-5114. Silicon rectifiers CR1 through CR4 and electrolytic capacitors C1 and C2 provide unregulated dc to series-pass transistor Q1 and regulator U1. This regulator sets the reference and gain.

Component designators are screened on the printed circuit board to aid in troubleshooting. If desired, the power supply assembly may be replaced as a unit.

23.2.3 Power Supply 3 (HC5-700)

Refer to schematic 03-174-5012. This power supply generates a dc voltage of +6V and is fed by split primary transformer T1. Silicon rectifiers CR1 through CR4 and electrolytic capacitor C3 provide unregulated dc to regulator U1. In conjunction with Q2, this regulator sets the reference and gain. Increased power output is provided by series-pass transistor Q1.

Component designators are screened on the printed circuit board to aid in troubleshooting. If desired, the power supply assembly may be replaced as a unit.

23.2.4 Power Supply Shutdown During Standby

When the power switch is in the Standby position, the −12.6V supply is connected through S1 (see mainboard schematic 03-004-5429) and 10K resistors R7, R8 and R9 to pin 13 of U1 on all three power supply boards (PS1, PS2 and PS3). The negative voltage at these three points disables the +5.4, +6 and +28V power supplies.

23.3 SPECIFICATIONS

The specifications for power supplies 1, 2, and 3 are as follows:

Power Supply 1 (HCC512-501)

Output Voltages	+5.4V at 1.5 amps. −12.4V at 0.5 amps. +23V at 150 mA.
Line Regulation	±0.05% for 10% line change.
Load Regulation	±0.05% for 10% line change.
Ripple	5 mVp-p maximum.

Overload Protection	Automatic current foldback.
Overvoltage Protection	+5.4V output only.
Temperature Rating	0 to +50°C, derated linearly to 40% at 70°C.
Efficiency	45%.

Power Supply 2 (MAA-500)

Input Voltage (for specified output)	Vrms = [V(dc output) +7.9V] × 0.707.
Output Voltage	+28V at 100 mA.
Line Regulation	±0.05% for 10% line change.
Load Regulation	±0.05% for 50% load change.
Ripple	5 mVp-p maximum.
Transient Response	30 μsec for 50% load change.
Overload Protection	Automatic current foldback.
Temperature Rating	100% at 0 to +50°C, 70% at 60°C, 40% at 70°C.
Stability	±0.1% for 8 hours after warm-up.

Power Supply 3 (HC5-700)

Output Voltage	+6V at 1.9 amps
Line Regulation	±0.05% for 10% line change.
Load Regulation	±0.05% for 50% load change.
Ripple	5 mVp-p maximum.
Overload Protection	Automatic current limit.
Overvoltage Protection	Set at +6.8V ±0.4V.
Temperature Rating	0 to +50°C, derated linearly to 40% at 70°C.
Efficiency	45%.

23.4 MAINTENANCE

23.4.1 Preventive Maintenance

Preventive maintenance is not required for any of the three power supply modules. Normal operation is indicated by the presence of correct outputs.

23.4.2 Alignment/Calibration

Field or customer alignment of these assemblies is not advised. If realignment is required, return the entire instrument to the factory for service.

23.4.3 Troubleshooting

Section 5 of this manual provides signal and test point information to isolate the problem to a faulty assembly. It is important to follow the procedures given in the troubleshooting table to ensure that all of the inputs are present, and that outputs are not correct before assuming an assembly to be faulty.

If any of the three power supply modules have been isolated as the source of the problem, the only authorized service is to return the entire instrument to the factory for repair.

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ZONE	LTR	ECO NO.	CHANGED BY	APPR'D BY	DATE
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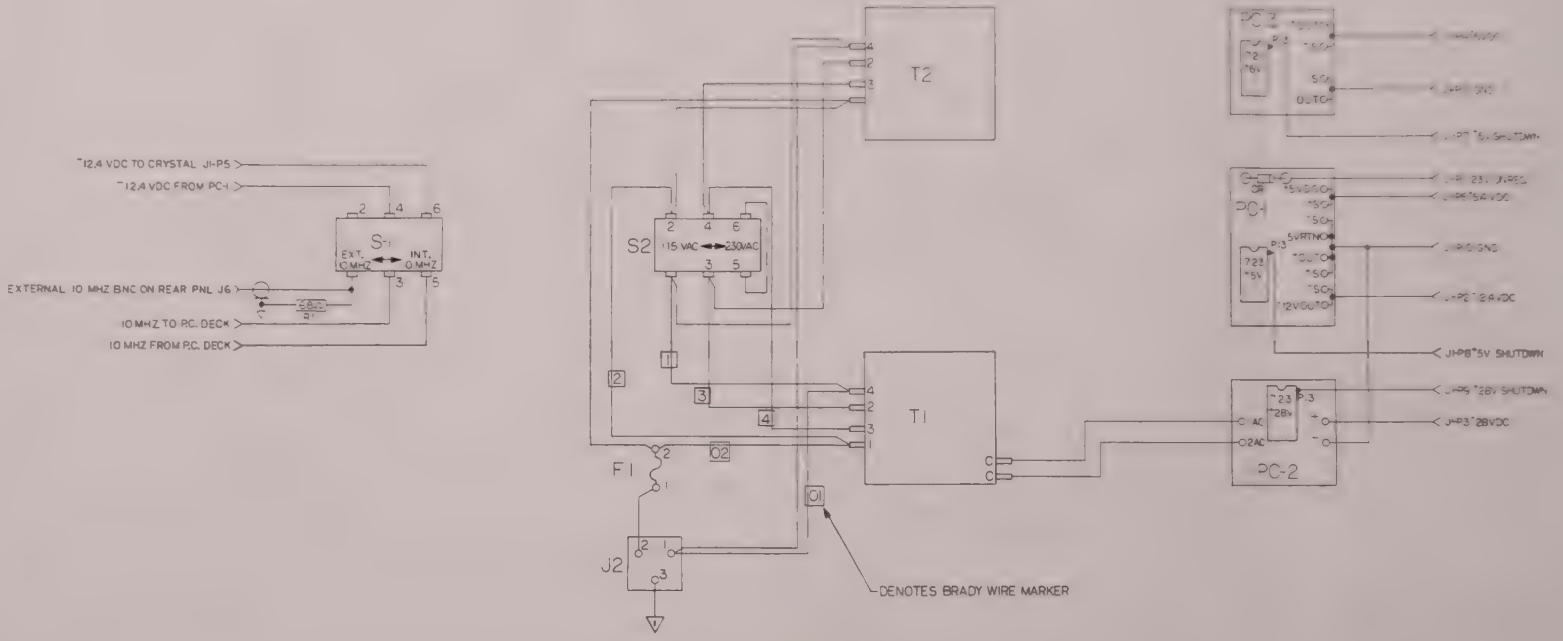
	B	2093			



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: MATERIAL — FINISH —

DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES

DRAWN — DATE 2-83 CHKD — ENG APPR — MFG APPR — ISSUED

WAVETEK ROCKLAND Wavetek Rockland, Inc.

TITLE: WIRING DIAGRAM REAR PNL AC WIRING

SIZE D — MODEL NO. — DRAWING NO. — REV B

SCALE NONE — SHEET — OF

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ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
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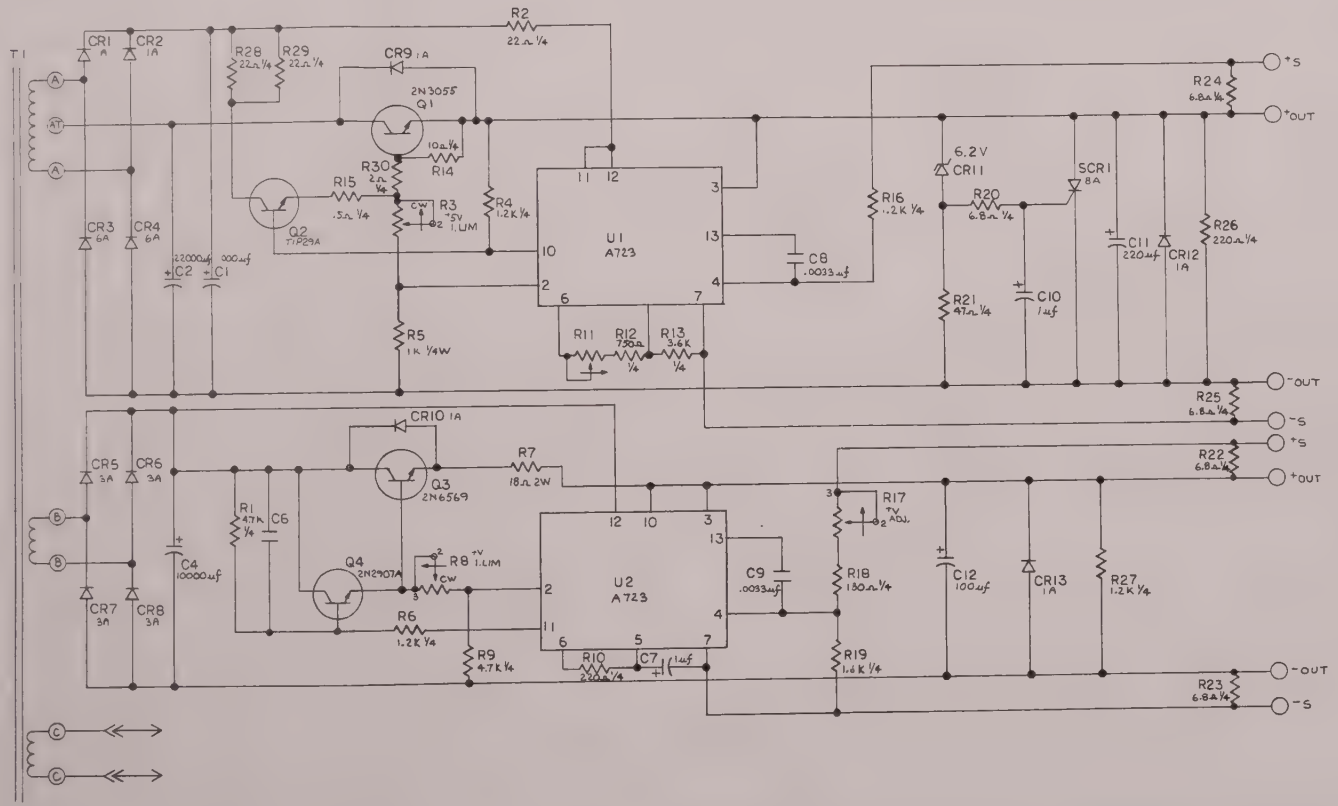
	B	2014	M.McMINN		9/11/85
	C	2017	M.McMINN		9/16/85



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	.xxx	.xx	∠
±1/64	±.005	±.01	±1°

MATERIAL: SHEET 2&3 "A" SIZE

FINISH: //

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN	JP	8-26-83
CHKD		1/3/84
ENG APPR.		1/20/84
MFG APPR.		1/23/84
ISSUED		

WAVETEK ROCKLAND Wavetek Rockland, Inc.

TITLE: SCHEMATIC POWER SUPPLY HCC512-501

SIZE	MODEL NO.	DRAWING NO	REV
C	5150	03-174-5013	C

SCALE: NONE | CODE IDENT 50621 | SHEET 1 OF 1

R.S. KNAPP

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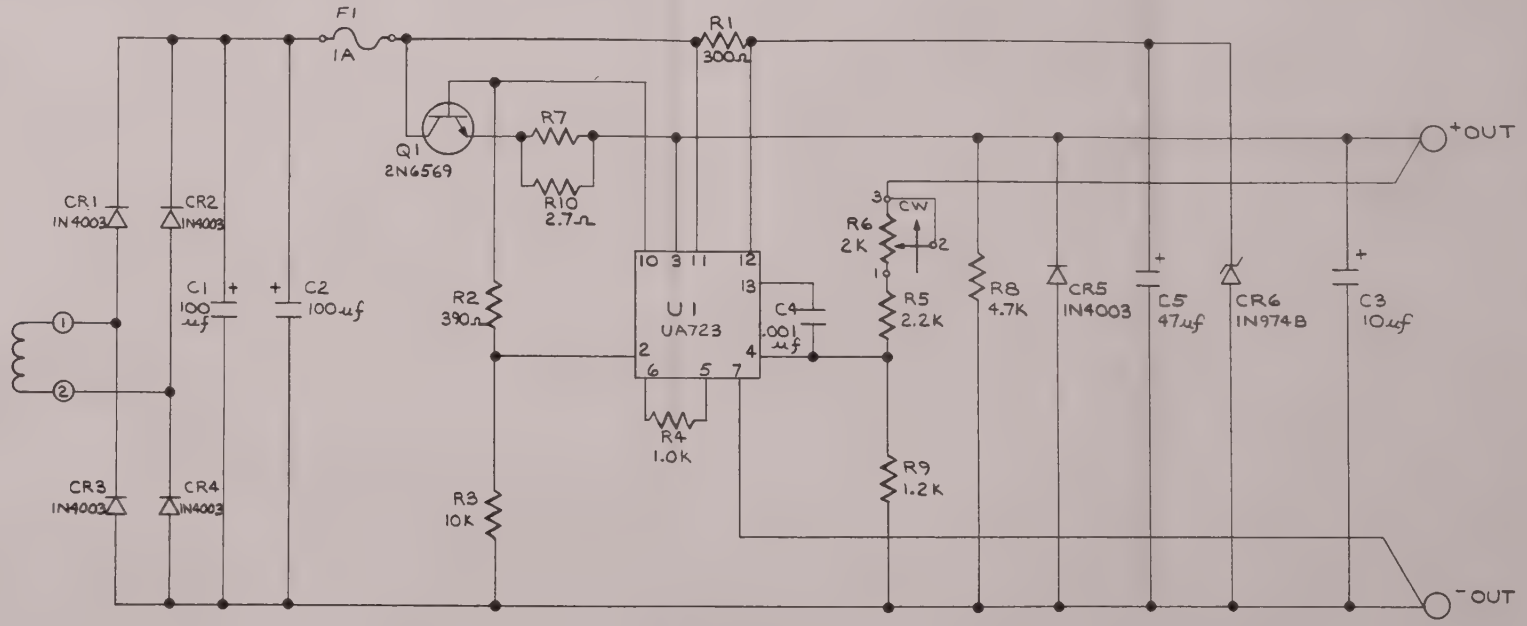
	A	RELEASE			10/17/85



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES
x/x ± 1/64	.xxx ± .005	.xx ± .01	∠ ± 1°	
MATERIAL SEE 02-174-5114				DRAWN JP 5/3/84
				CHKD
				ENG APPR. 10/17/85
FINISH				MFG APPR.
				ISSUED

WAVETEK
Wavetek Rockland Scientific, Inc

TITLE: SCHEMATIC POWER SUPPLY MAA-500

SIZE	MODEL NO	DRAWING NO	REV
B	5150	03-174-5114	A

SCALE: NONE | CODE IDENT 50621 | SHEET 1 OF 1

R.S.Knapp 822

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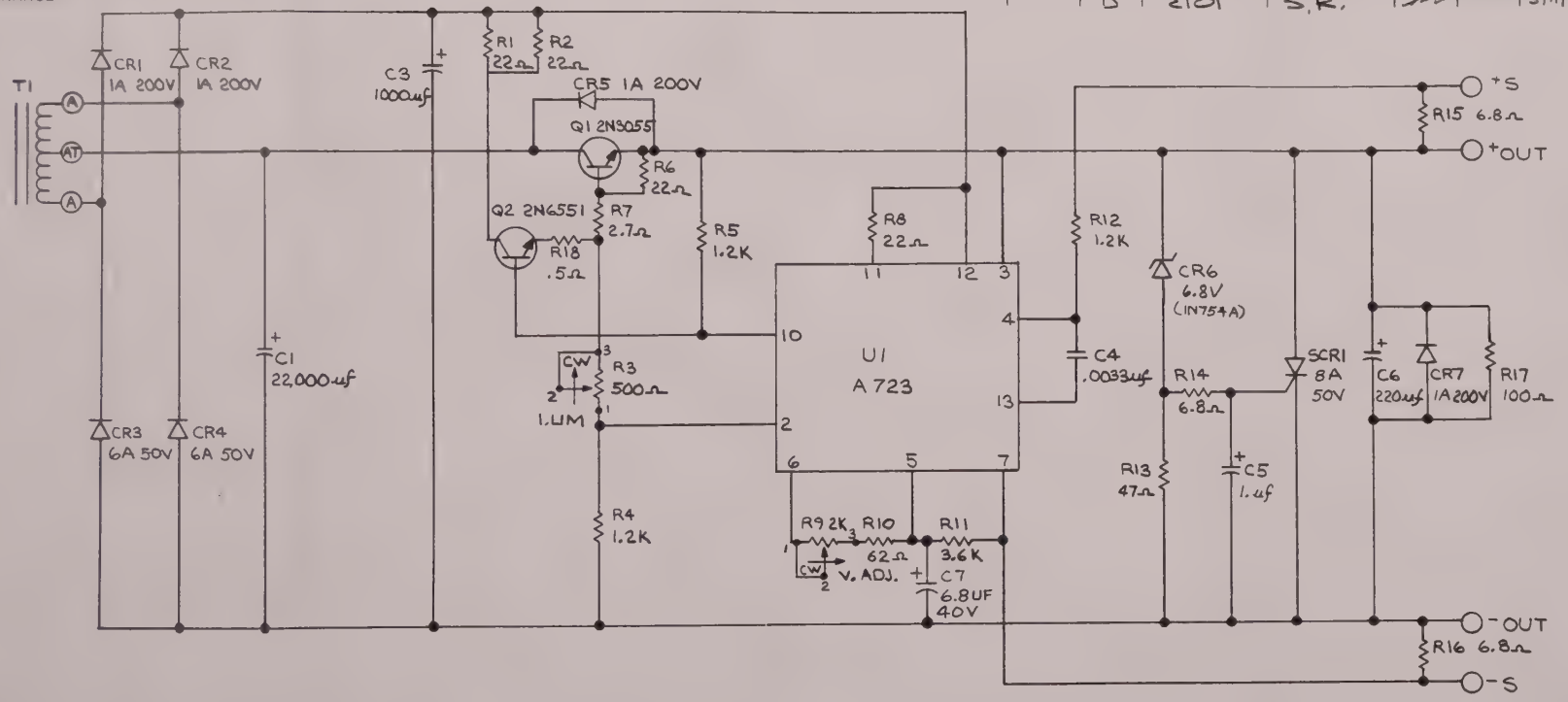
ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
	A	RELEASE			1/23/84
	B	1706			5/17/84
	C	2013	M.McMINN		9/11/85
	D	2101	S.R.		3/11/86



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x ±1/64	.xxx ±.005	.xx ±.01	∠ ±1°

MATERIAL: SHEET "2" "A" SIZE

FINISH: ——//——

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN	JP	8-29-83
CHKD		1-23-84
ENG APPR.		1/23/84
MFG APPR.		1/25/84
ISSUED		

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: SCHEMATIC POWER SUPPLY HC5-700

SIZE	MODEL NO.	DRAWING NO	REV
B	5150	03-174-5012	D

SCALE: NONE | CODE IDENT 50621 | SHEET 1 OF 1

RS KNAPP

SECTION 24
MODEL 5155A/5156A ELECTRICAL OPTIONS

24.1 INTRODUCTION

Options 001, 002 and 004 are internal, high stability crystal controlled oscillators operating at 10.000000 MHz. Options 001 and 004 are "oven-type" oscillators with an output voltage of 1.0 Vrms into 50 ohms. Option 004 has the best stability of the three oscillators. Option 002 is an internal temperature compensated oscillator with an output voltage of 0.5 Vrms into 50 ohms.

Option 003 (5155A only) routes the RF signal from the output amplifier module to a rear panel BNC-type jack instead of the front panel "N" type jack. Routing of the RF signal to the rear panel is standard on the Model 5156A.

Option 006 allows the user to remotely program the instrument over the IEEE-488 bus (also called the GPIB, General Purpose Interface Bus). The standard BCD (Binary Coded Decimal) interface can also be used to remotely program the instrument.

24.2 THEORY OF OPERATION

24.2.1 IEEE-488 Interface (Option 006 for Model 5155A Only)

Refer to schematic 03-004-5414. For the IEEE-488 interface, most of the protocol functions are handled by the General Purpose Interface Adapter (GPIA). This is a single IC (U1) that meets all the handshaking requirements of the 1978 IEEE-488 standard. Data and control portions of the bus require high current driving capability and specific line termination provided by bus drivers, U2 and U3. When there is a pending interrupt, IRQ (U1 pin 40) is asserted low. This alerts the microprocessor of an interrupt condition, causing it to interrogate the eight registers internal to U1. Data from the IEEE-488 bus (listen mode) is accessed by reading from the data registers in U1. Data output (talk mode) is written to the same register location.

The DIP address switch located on the rear panel (S1), selects the GPIB address for the instrument. Pull-up resistors (U5) hold input lines to U4 high unless S1 pulls one or more of these lines low. The address strobe enable line (ASE) from U1 can disable the output of U4, and therefore, S1. The microprocessor reads the switch by interrogating data lines D0 through D7 from U4.

24.2.2 IEEE-488 Interface (Option 006 for Model 5156A Only)

When properly addressed from the IEEE bus, the IEEE interface board (schematic 03-004-5416) converts amplitude data from either the BCD or IEEE bus to a voltage capable of driving the output attenuator in the RF section of the unit. It also provides frequency data interfacing between the IEEE connector and the front panel board.

The IEEE interface board sets amplitude to zero during initial power up. If J1 (BCD) is not connected and the unit is not programmed by the IEEE bus, the output voltage will go full scale when a frequency is loaded.

When frequency data is sent over the IEEE data bus, the IEEE interface board detects the first character, "F", and alerts the front panel board. Numerical data, the decimal point ("DP"), megahertz ("M") and kilohertz ("K") are then decoded by the interface board and sent to the front panel board.

The IEEE paddle board interface (shown in schematic 03-009-9546) connects the IEEE portion of the interface board to the rear panel connector and contains the address DIP switch used to select the instrument address.

For a more detailed description, refer to "IEEE-488 (Option 006) For 5156A" located in paragraph 6.2.2.

24.3 SPECIFICATIONS

24.3.1 Option 001 (High Stability Crystal Oscillator)

The high stability (proportional oven controlled) crystal oscillator, Option 001, has the following specifications at the oscillator output. For rear panel output voltage, see paragraph 1.2.1.

Operating Frequency	10.000000 MHz.
Aging	$\pm 4 \times 10^{-9}$ per year.

Output Voltage	1.0 ± 0.3 Vrms into 500Ω.
Temperature Stability	$\pm 1 \times 10^{-8}$ 0° to 50°C.
Warm-up Time	24 hr for 1×10^{-8}
DC Supply	−12.4V at 250 mA (500 mA start-up).

24.3.2 Option 002 (Standard Crystal Oscillator)

The standard stability (temperature compensated) crystal oscillator, Option 002, has the following specifications at the oscillator output. For rear panel output voltage, see paragraph 1.2.1.

Operating Frequency	10.000000 MHz.
Aging	$\pm 4 \times 10^{-6}$ per year.
Output Voltage	1.0 ± 0.3 Vrms into 500Ω.
Temperature Stability	$\pm 1 \times 10^{-6}$ 0° to 50°C.
DC Supply	−12.4V at 20 mA.

24.3.3 Option 004 (Very High Stability Crystal Oscillator)

The very high stability (proportional oven controlled) crystal oscillator, Option 004, has the following specifications at the oscillator output. For rear panel output voltage, see paragraph 1.2.1.

Operating Frequency	10.000000 MHz.
Aging	$\pm 5 \times 10^{-10}$ per year.
Output Voltage	1.0 ± 0.3 Vrms into 500Ω.
Temperature Stability	$\pm 1 \times 10^{-8}$ 0° to 50°C.
Warm-up Time	24 hr for 1×10^{-8}
DC Supply	−12.4V at 250 mA (500 mA start-up).

24.3.4 Option 006 (GPIB Interface—Model 5155A only)

This option meets all electrical specifications of IEEE-488 (1978) including the following bus and physical characteristics.

Card Configuration	Paddle board construction.
Interface Controller	MC68488.
Address Control	One 8-section DIP switch.
Bus Management	Bidirectional IEEE-488 to Z-80.
DC Supply	+5.4V at 150 ma.
Connectors	One 26-pin IDC (internal). One 24-pin GPIB (external).

24.3.5 Option 006 (GPIB Interface—Model 5156A only)

The option 006 for the Model 5156A consists of two separate boards and meets all of the specifications of IEEE-488 (1978).

9546 Board

Card Construction	Paddle-board.
Address Control	One 8-section DIP switch.
Connectors	One 26-pin IDC (internal). One 24-pin GPIB (external).

5416 Board

Bus Management	Unidirectional IEEE-488 to BCD format.
Internal Signals	1, 2, 4, and 8 BCD (negative true). High = +3.0V minimum. Low = +0.5V maximum.
External Signals	IEEE-488 Bus.
DC Supply	+5.4V at 380 mA. −12.4V at 10 mA. +23V at 10 mA.
Connectors	One 34-pin right-angle IDC. Two 14-pin IDC. Two 30-pin edgecard.

24.4 MAINTENANCE

24.4.1 Preventive Maintenance

The only preventive maintenance for options 001, 002 and 004 is to maintain constant power at the oscillator circuitry when not using the instrument (front panel power switch to "Standby" with power cord connected) and calibration of the crystal oscillator as described in paragraph 24.4.2. Normal operation is indicated for options 001, 002 and 004 by the correct nominal 10 MHz output frequency and amplitude.

Preventive maintenance is not required for options 003 and 006. Normal operation is indicated for option 003 by correct output frequencies and levels. GPIB bus commands of the correct level and timing indicate normal operation of option 006.

24.4.2 Alignment/Calibration

Options 001, 002 and 004

Base the calibration interval on the instrument application and aging rate of the oscillator.

A high accuracy frequency counter is required for oscillator frequency calibration. The Hewlett Packard Model 5315 or similar counter is suggested for use. For highest accuracy, connect an external frequency standard derived from WWV to the counter's time base input. The Spectracom Model 8161 standard frequency receiver/oscillator may be used for this purpose.

Use the following procedure to calibrate the crystal oscillator output frequency.

NOTE

Connect a 10 MHz external primary or secondary standard to the external time base frequency counter input. If a frequency standard is not available, do not attempt to adjust the 10 MHz frequency unless the counter being used has the accuracy needed to make the adjustment.

1. Connect the 10 MHz OUT connector on the 5155A/5156A rear panel to the counter input connector. If frequency is within the required specification and adjustment is *not* needed, move to step 5.
2. Locate the oscillator assembly (see figure 5-2) and remove the cover screw.
3. Set the oscillator frequency for 10 MHz with the required accuracy.
4. Replace the cover screw.
5. Record the 10 MHz setting for future reference.

Option 003

There are no adjustments to be made for option 003 as used in the Model 5155A.

Option 006

Field or customer alignment of option 006 is not feasible nor advised. If realignment is required, return the entire instrument to the factory for service.

24.4.3 Troubleshooting

Option 006

Since the interface was exhaustively tested prior to shipment, the probability is low that problems encountered when first setting up the system are due to hardware failures. It is more likely that some set-up parameter, device address, or software convention is causing the problem.

If the system has been successfully operating for some time and then fails with no system changes having been made, a hardware failure may be indicated.

In the event that the bus system is not performing correctly, many functional tests may be made to help locate the cause. In general, an effort should be made to reduce both the hardware and software complexity of the system to the simplest configuration which still exhibits the problem.

Check List of Setup Problems

Before attempting diagnostic tests, the following list of common set-up errors should be checked:

1. Make sure that power is applied to all of the units connected to the bus system.
2. Check the tightness of the bus cable connectors. A connector which is not secured by the captive screws may become partially disengaged from its mating socket causing intermittent or open connections.
3. Review the address code structure of the system making sure that no two devices unintentionally share the same address code. Make sure the controller is correctly identifying each device by its respective address.

Diagnostic Tests

Problems can generally be classified as either related to the bus system operation or to the synthesizer itself. The controller is usually provided with some fault-indicating messages which can be useful in diagnosing the bus problems.

1. Bus Testing

   The most basic bus activity is the handshake function which is required for all universal commands and data transfers. The controller will generally indicate if there is a problem in completing the handshake. If a problem exists, the offending device can be determined by connecting devices to the bus one at a time.

   The next level of activity is establishing the various devices as active listeners of talkers. The synthesizer indicates its status by the green *Listen* lamp. Each bus device should respond appropriately to the universal commands and not interfere with each other. A unit-by-unit check of these operations will verify correct performance of these functions.

2. IEEE Interface Testing

   If the bus activity appears normal but data is not being loaded correctly into the synthesizer, make sure that the "LF, CR" or "GET" command is being issued by the controller. In addition, the green Remote lamp on the front panel of the synthesizer must be lit during remote transfers. If not, check that the REMOTE ENABLE line on the bus is sent active by the controller.

Hardware Testing

If the above tests have not uncovered the problem, troubleshooting of the hardware may be required. The information in paragraphs 24.2.5 and 24.2.6 along with the schematic diagrams may be used. Careful use of printed circuit repair techniques may be used when replacing faulty components if either the IEEE interface or paddle board is isolated as the source of the problem.

If the Z80, front panel or IEEE board has been isolated as the source of the problem, the only authorized service is to return the entire instrument to the factory for repair.

Factory Assistance

If the problem cannot be remedied by these procedures, factory assistance can be obtained by calling or writing:

Applications Engineering
Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007

Before returning a unit to the factory for repair, authorization from Customer Service must be obtained. A written description of the problem and any related symptoms will assist our repair technicians in making a complete and prompt repair.

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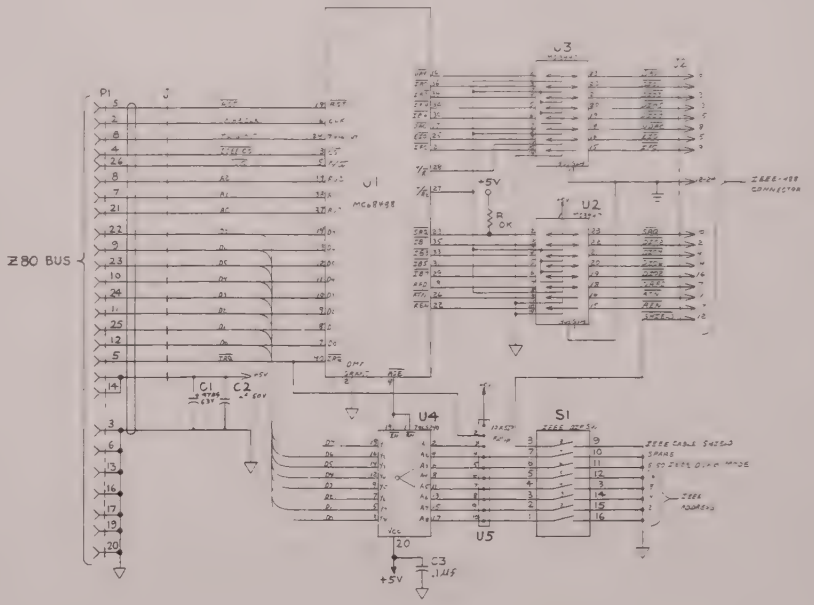

DESIG	-5V	GND

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES

DRAWN R.M. 11-7-84

CHKD

ENG APPR. 11/8/84

MFG APPR.

ISSUED

MATERIAL

FINISH

WAVETEK ROCKLAND Wavetek Rockland, Inc.

ELECTRICAL SCHEMATIC
IEEE 488 INTERFACE

SIZE	DWG NO.	REV
D	03-004-5414	A

SCALE — CODE IDENT 23338 SHEET 1 OF 1

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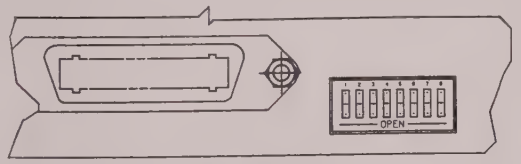
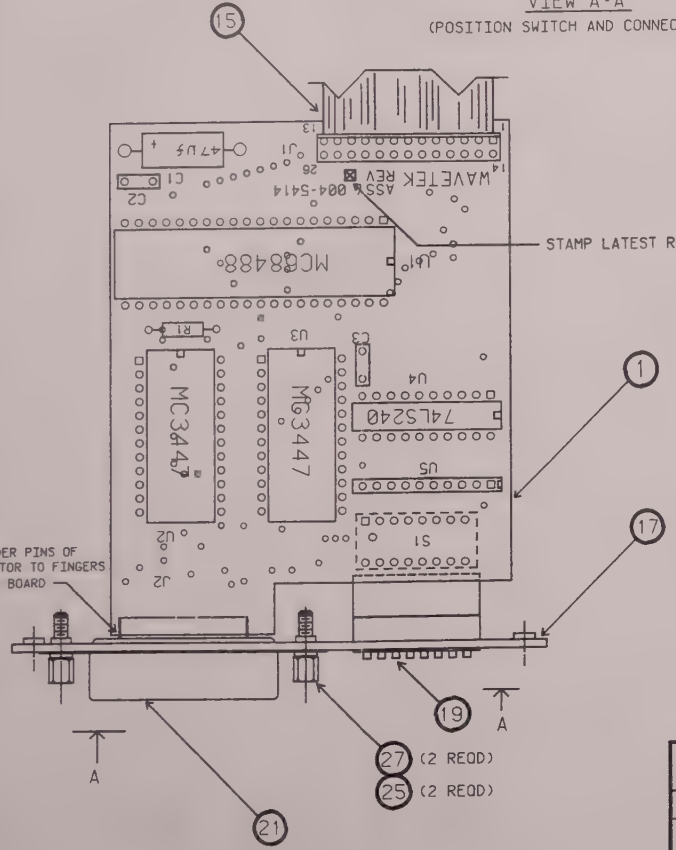
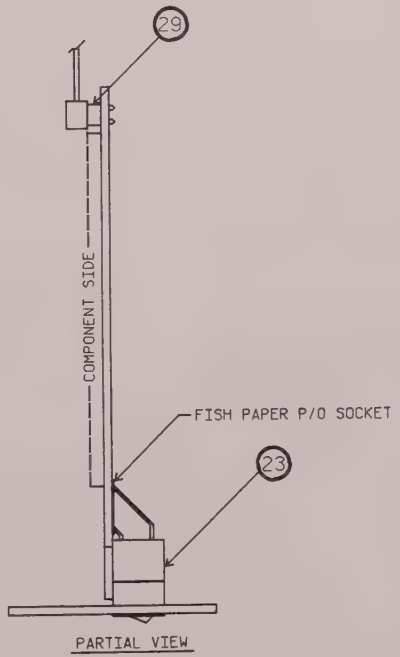
ZONE	LTR	ECO BY	CHANGED BY	APPRD BY	DATE
	A	RELEASE			



VIEW A-A
(POSITION SWITCH AND CONNECTOR AS SHOWN)





PARTIAL VIEW

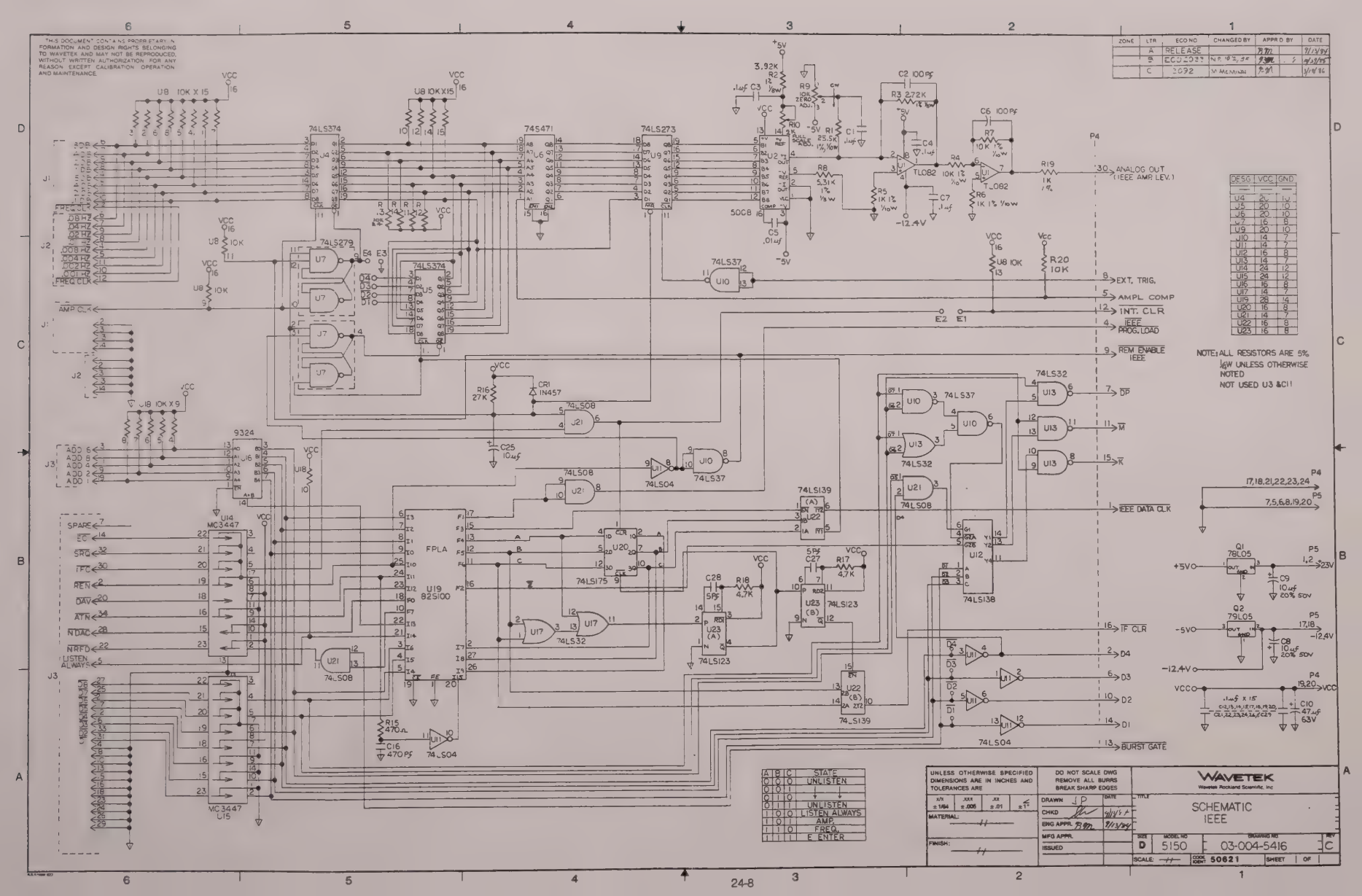
SHEET 2 OF 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: X/X ±1/64, .XXX ±.005, .XX ±.01, ∠ ±1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific, Inc.
MATERIAL: #	DRAWN M. MCMINN 4/26/84	TITLE: P. C. ASSEMBLY IEEE 488 INTERFACE
FINISH: #	CHKD	
	ENG APPR. 11/3/84	
	MFG APPR.	SIZE C · MODEL NO. 5150 · DRAWING NO. 02-004-5414 · REV A
	ISSUED	SCALE: 2:1 · 50621 · SHEET 1 OF 2

WAVETEK SD INC. .DWG NO. 02 004 5414 REV A

PC ASSY: IEEE INTERFACE

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: IEEE INTERFACE, 5150 STD	320.5414	1.00
3	U2,U3	U: IEEE BUS XCVR (MC3447P)	120.2447	2.00
5	U4	U: OCT BUF INV 3-ST (74LS240)	125.0144	1.00
7	U5	U: PULL UP NET 10K 2% X9 SIP	128.3104	1.00
9	U1	U: MC68488-MH	129.3202	1.00
11	C2,C3	C: FX MONO 0.1UF Z5U 50V	100.4102	2.00
13	C1	C: FX ELECT 47UF 20% 63V	109.6470	1.00
15	-	CABLE ASSY: 5150 RP/Z-80 (STD)	009.9545	1.00
17	-	CONN MTG PLATE: IEEE 5150 STD	303.0914	1.00
19	S1	S: DIP 8 POLE 2 POS	342.8100	1.00
21	J2	CONN: RIB SKT CHASSIS 24 CNT	351.2403	1.00
23	-	SOCKET: IC 16PIN DIP HOR	353.1605	1.00
25	-	WASHER: SPLT LK STNLS #8	388.1082	2.00
27	-	GUIDE PIN ASSY FEM METRIC	[illegible]	2.00
29	-	CONN: TERM 50PIN DIL ST	354.0021	1.00
31	R1	R: FX CFLM 10K OHM 5% 1/4W	116.3101	1.00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ZONE | LTR | ECO NO | CHANGED BY | APPR'D BY | DATE
A | RELEASE | | | 7/13/84
B | ECO 2029 | | | 10/5/84
C | 2092 | | | 1/14/86
DESG | VCC | GND
NOTE: ALL RESISTORS ARE 5% 1/8W UNLESS OTHERWISE NOTED
NOT USED U3 & C11
ANALOG OUT (IEEE AMP LEV.)
EXT. TRIG.
AMPL COMP
INT. CLR
IEEE PROG. LOAD
REM ENABLE IEEE
IEEE DATA CLK
IF CLR
D4
D3
D2
D1
BURST GATE
74LS374
74LS273
74LS279
74LS37
74LS32
74LS08
74LS04
74LS139
74LS138
74LS123
74LS175
74LS74
74LS00
9324
MC3447
FPLA
82S100
TL082
TL071
78L05
79L05
SPARE
SRQ
IFC
REN
DAV
ATN
NDAC
NRFD
LISTEN ALWAYS
A B C STATE
0 0 0 UNLISTEN
0 0 1
0 1 0
0 1 1 UNLISTEN
1 0 0 LISTEN ALWAYS
1 0 1 AMP.
1 1 0 FREQ.
1 1 1 E ENTER
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES
MATERIAL:
FINISH:
DRAWN
CHKD
ENG APPR.
MFG APPR.
ISSUED
WAVETEK
Wavetek Rockland Scientific, Inc
TITLE
SCHEMATIC
IEEE
SIZE D
MODEL NO 5150
DRAWING NO 03-004-5416
REV C
SCALE:
CODE IDENT NO 50621
SHEET OF
24-8

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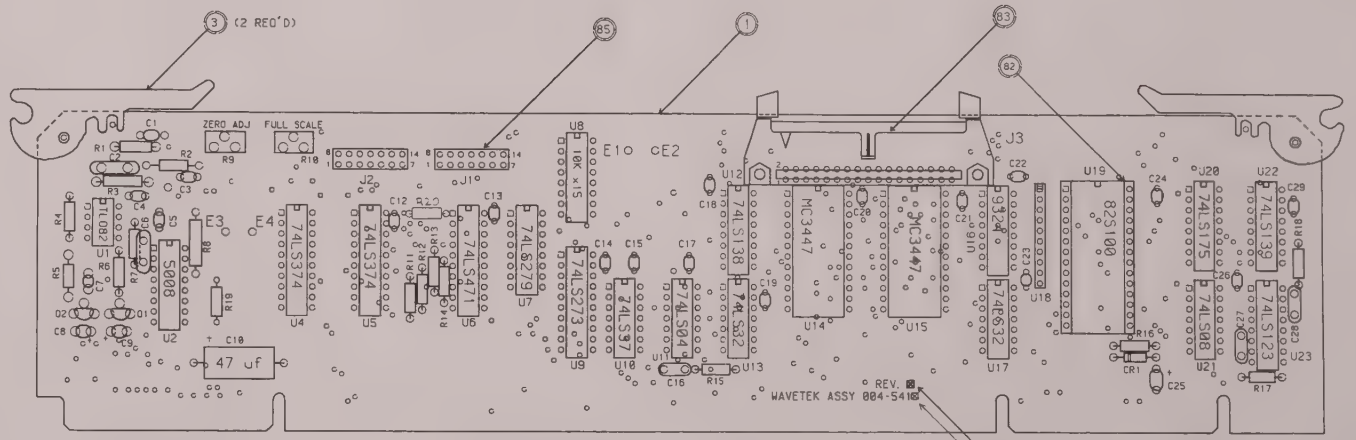
ZONE	LTR	ECO NO	CHANGED BY	APPRD BY	DATE



SHEETS 2 TO 4 ARE "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE X/X ±1/64 · .XXX ±.005 · .XX ±.01 · ∠ ±1 MATERIAL FINISH	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES DRAWN PETERS 8/12/84 CHKD ENG APPR. 9/1/84 MFG APPR ISSUED	WAVETEK Wavetek Rockland Scientific, Inc. TITLE P.W.B. ASSEMBLY IEEE SIZE D · MODEL NO 5150 · DRAWING NO. 02 - 004 - 5416 F SCALE 2:1 · 50621 · SHEET 1 OF 4

WAVETEK SD INC. DWG NO. 02-004-5416 REV F

PC ASSY: IEEE (5156A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: IEEE INTERFACE, REM, 5150	320.5416	1.00
3	-	EJECTOR: PC, 5155A	364 0404	2.00
5	U11	U: HEX INVERTER	125.7404	1.00
7	U21	U: QUAD 2 IN AND GATE	125.7408	1.00
9	U17,U13	U: QUAD 2 IN OR GATE	125.7432	2.00
11	U4,U5	U: OCT D-FLIP 3-ST (74LS374)	125.0140	2.00
13	U7	U: QD S-R LATCH (74LS279)	125.0129	1.00
15	U23	U: DL MNSTBL MULTVIB (74LS123)	125.0107	1.00
19	U22	U: DL 2TO4 LN DECOD 74LS139	125.0116	1.00
21	U12	U: 3 TO 8 LINE DECOD (74LS138)	125.0115	1.00
23	U20	U: QUAD D FLIP-FLOP (74LS175)	125.0118	1.00
25	U10	U: QUAD 2 IN NAND BUFFER	125.7437	1.00
27	U9	U: OCT D-FLIP W/CLR (74LS273)	125.0139	1.00
29	U6	PROM: PGMD U6-5416 (129.3012)	021.1025	1.00
33	U16	U: 5 BIT COMPARATOR	122.9324	1.00
35	U14,U15	U: IEEE BUS XCVR (MC3447P)	120.2447	2.00
37	U19	FPLA: PGMD 5150	022.0005	1.00
39	U2	DAC: 8 BIT BINARY	129.1505	1.00
41	U1	U: DL LIN BIFET OP-AMP (TL082C	120.2082	1.00
43	Q1	Q: P.V. REG 5V (78L05)	120.0053	1.00
45	Q2	Q: N.V. REG 5V (79L05)	120.0054	1.00
47	CR1	CR: SL LW LK 70PIV 200MW 1N457	132.0457	1.00
[illegible]	C27,C28	C: FX MICA DP 5PF +-.5PF 500V	101.0050	2.00
51	C16	C: FX MICA DP 470PF +-5% 500V	101.1470	1.00
53	C2,C6	C: FX MICA DP 100PF +-5% 500V	101.1100	2.00
55	C5	C: FX MONO .01UF +80 -20% 50V	100.3105	1.00
57	C1,C3,C4,7 ,12,13,14,15,17,	C: FX MONO 0.1UF Z5U 50V	100.4102	18.00
57	C18,19,20,21,22,23,24,26,29	C: FX MONO 0.1UF Z5U 50V	100.4102	0.00
59	C25	C: FX TANT 10UF 20% 20V	109.6100	1.00
60	C10	C: FX ELECT 47UF 20% 63V	109.6470	1.00
61	C8,C9	C: FX TANT 10UF 20% 50V	109.6101	2.00
62	R10	R: VAR CMT 2.0K 3/8SQ EM	118.2203	1.00
63	R9	R: VAR CMT 10K 3/8SQ EM	118.3103	1.00
65	R5,R6,R19	R: FX MFLM 1.00K 1% 1/10W T2	111.1001	3.00
66	R11,R12,R13,R14,R20,	R: FX CFLM 10K OHM 5% 1/4W	116.3101	5.00
67	R15	R: FX CFLM 470 OHM 5% 1/4W	116.1471	1.00
69	R3	R: FX MFLM 2.72K 1% 1/8W T0	111.2720	1.00
71	R7,R4	R: FX MFLM 10.0K 1% 1/10W T2	112.1001	2.00
72	R1	R: FX MFLM 25.5K 1% 1/10W T2	112.2551	1.00
73	R17,R18	R: FX CFLM 4.7K OHM 5% 1/4W	116.2471	2.00
75	R2	R: FX MFLM 3.92K 1% 1/10W T2	111.3921	1.00

WAVETEK SD INC. DWG NO. 02-004-5416 REV F

PC ASSY: IEEE (5156A)

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
77	R8	R: FX MFLM 5.31K 1% 1/8W T0	111.5310	1.00
79	R16	R: FX CFLM 27K OHM 5% 1/4W	116.3271	1.00
82	FOR U19	SOCKET: IC 28PIN DIP ST	353.2800	1.00
83	J3	PLUG: HDR 34P DIL RT ANG ST LK	352.3400	1.00
85	J1	CONN: TERM 4 PIN SIL ST	354.0037	1.00
87	U18	U: PULL UP NET 10K 2% X9 SIP	128.3104	1.00
89	U8	U: PULL UP NET 10K 2% X15	128.3101	1.00

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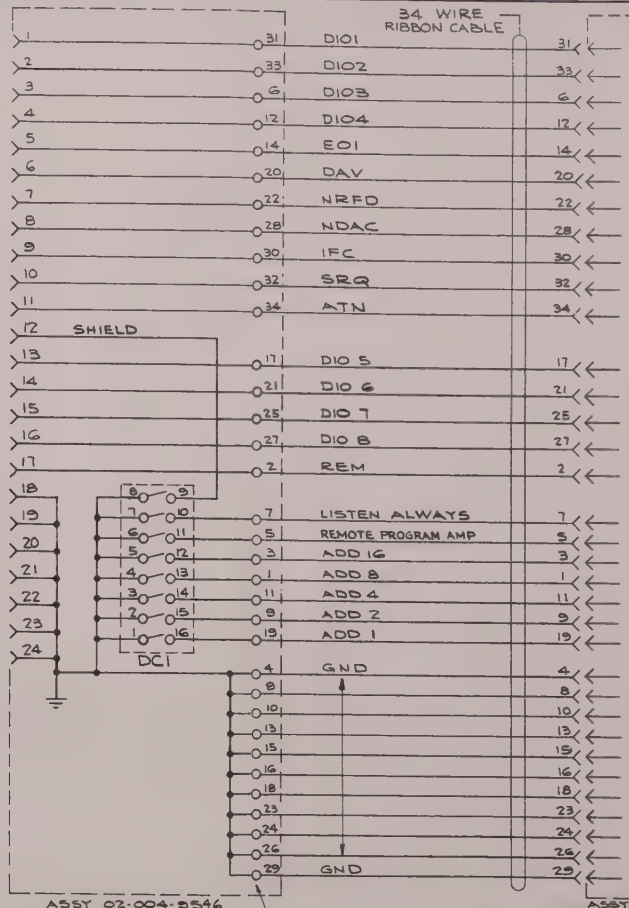
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			3/19/86



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

X/X	.XXX	.XX	∠
±1/64	±.005	±.01	±1°

MATERIAL: —

FINISH: —

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN	S.E	3/19/86
CHKD	[illegible]	3/19/86
ENG APPR.	[illegible]	3/19/86
MFG APPR.		
ISSUED		

WAVETEK ROCKLAND Wavetek Rockland, Inc.

TITLE: ELECTRICAL SCHEMATIC IEEE PADDLE BOARD INTERFACE

SIZE	MODEL NO.	DRAWING NO.	REV
C	5130	03-009-9546	A

SCALE: — CODE IDENT 23338 SHEET 1 OF 1

K.S. KNAPP

WAVETEK SD INC. DWG NO. 02 009 9546 REV A

CABLE ASSY: RP/IEEE

ITEM	REFERENCE DESIGNATORS	DESCRIPTION	PART NO.	QUANTITY
1	-	PWB: PADDLE BD IEEE (751/752)	320.0775	1.00
3	-	CONN MTG PLATE: IEEE 5150 REM	303.0913	1.00
5	-	CONN: RIB SKT CHASSIS 24 CNT	351.2403	1.00
7	-	CONN: BD/CABLE 34CONT .050	354.3400	1.00
9	23"	CABLE: 34CND RIB 28GA STR .050	378.4018	1.00
11	-	SOCKET: 34PIN DIL LOCK CLSEND	353.3402	1.00
13	-	SOCKET: IC 16PIN DIP HOR	353.1605	1.00
15	DC1	S: DIP 8 POLE 2 POS	342.8100	1.00
17	-	GUIDE PIN ASSY FEM METRIC	389.7004	2.00
19	-	WASHER: SPLT LK STNLS #8	388.1082	2.00

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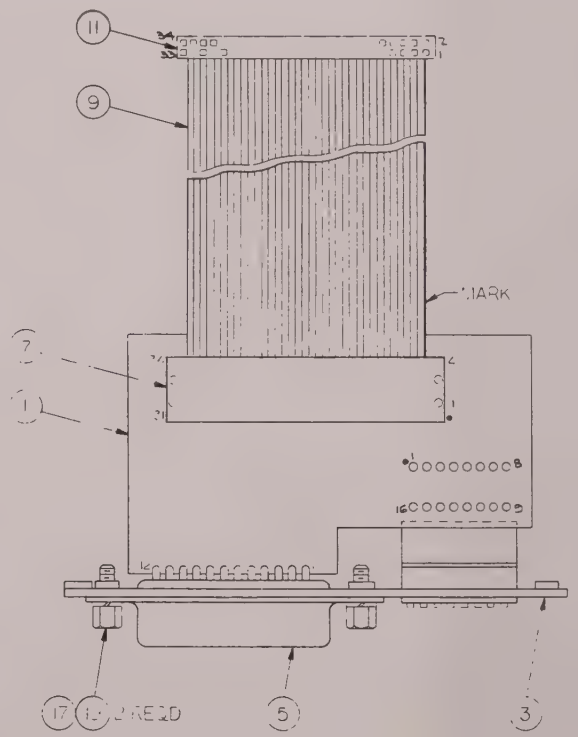
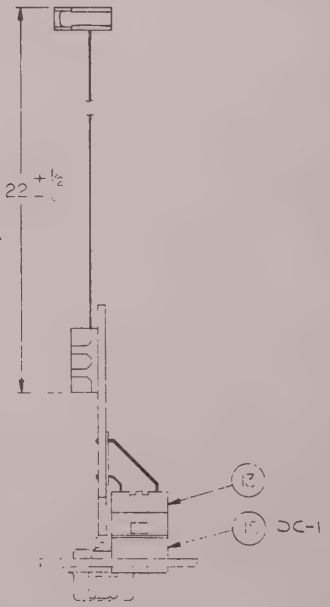
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE		





NOTE

1. ASSEMBLE ITEM 7, 9, AND 11 BEFORE INSTALLING ON P.C. BOARD.

SHT 2 IS A SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
x/x ±1/64 .xxx ±.005 .xx ±.01 ∠ ±1°	DRAWN: DATE 5-2-84	TITLE: IEEE PADDLE BOARD ASSEMBLY
MATERIAL —	CHKD	
	ENG APPR. 5/2/84	
FINISH: —	MFG APPR. 5/2/84	SIZE C · MODEL NO. 5150 · DRAWING NO. 202-009 - 9546 · REV A
	ISSUED	SCALE: 2:1 · CODE IDENT 23338 · SHEET 1 OF 2

R.B. KNAPP

APPENDIX A
AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)

b7 b6 b5 / BITS / b4 b3 b2 b1 / column / row	0_0	MSG[1]	0_1	MSG	0_2	MSG	0_3	MSG	1_0	MSG	1_1	MSG	1_2	MSG	1_3	MSG
0 0 0 0 / 0	NUL		DLE		SP	MLA ASSIGNED TO DEVICE	0	MLA ASSIGNED TO DEVICE	@	MTA ASSIGNED TO DEVICE	P	MTA ASSIGNED TO DEVICE	\	MEANING DEFINED BY PCG CODE	p	MEANING DEFINED BY PCG CODE
0 0 0 1 / 1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0 0 1 0 / 2	STX		DC2		"		2		B		R		b		r	
0 0 1 1 / 3	ETX		DC3		#		3		C		S		c		s	
0 1 0 0 / 4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0 1 0 1 / 5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0 1 1 0 / 6	ACK		SYN		&		6		F		V		f		v	
0 1 1 1 / 7	BEL		ETB		'		7		G		W		g		w	
1 0 0 0 / 8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1 0 0 1 / 9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1 0 1 0 / 10	LF		SUB		*		:		J		Z		j		z	
1 0 1 1 / 11	VT		ESC		+		;		K		[		k		{	
1 1 0 0 / 12	FF		FS		,		<		L		\		l		|	
1 1 0 1 / 13	CR		GS		-		=		M		]		m		}	
1 1 1 0 / 14	SO		RS		.		>		N		^		n		~	
1 1 1 1 / 15	SI		US		/		?	UNL	O		_	UNT	o		DEL	

ADDRESSED COMMAND GROUP (ACG)

UNIVERSAL COMMAND GROUP (UCG)

[4] LISTEN ADDRESS GROUP (LAG)

TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Addressed Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
BS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B

MODEL 5155A GPIB (IEEE-488) PROGRAMMING COMMAND SUMMARY (Excluding GPIB Command Groups Given in Appendix A)

Control and Data Names	ASCII Primary Command	ASCII Secondary Command	ASCII Minimum Command
Frequency	F[FREQUENCY	—	F
Amplitude	A[AMPLITUDE	—	A
Decimal Point	.	—	.
Numeric Data	0,1,2,...9	—	0,1,2,...9
Frequency Terminator	—	M[HZ	M
	—	K[HZ	K
	—	H[Z	H
	—	m[HZ*	m*
Amplitude Terminator	—	D[B	D
	—	V*	V*
	—	m[V*	m*
Display Modifier*			
On / Off*	M[ODIFY*	ON*	M ON*
	M[ODIFY*	OFF*	M OFF*
Modify digit — Up*	M[ODIFY*	U[P*	M U*
Modify digit — Down*	M[ODIFY*	D[OWN*	M D*
Modify digit — Left*	M[ODIFY*	L[EFT*	M L*
Modify digit — Right*	M[ODIFY*	R[IGHT*	M R*
RF Output*	RF*	ON*	RF ON*
	RF*	OFF*	RF OFF*
Execute*	E[XECUTE*	—	E*
Rev*	REV*	—	REV*
Command Recall*	REC[ALL*	—	REC*
Status*	S[TATE*	—	S*
Help*	H[ELP*	—	H*

* These commands are **not** available in the Model 5156A compatibility mode (see section 3.7.2.1) and will generate an SRQ if the 5156A compatibility mode switch (No. 7 on rear panel) is selectd.

NOTES TO PROGRAMMING COMMANDS

1. Rear panel switch (No. 7) forces the user to program the 5155A in commands that are acceptable to the 5156A. Any other commands will generate an SRQ.
2. Except for the m (milli), only capital letters may be used. A space is needed after each primary and secondary command as separators.
3. The required portion of each command is separated from the remainder of the command by the "[" symbol. If more than the minimum command is used, the word must follow the spelling as listed in the table. For example:

   "F", "FREQ", and "FREQUENCY" are all acceptable commands
   but "FREQUNCY" is not.

4. Numeric data for the FREQUENCY and AMPLITUDE commands may be entered in any format including scientific notation. In addition, the modifiers, M for 10^6, K for 10^3, H for 10^0, and m for 10^{-3} may be used in conjunction with scientific notation.

NOTES TO PROGRAMMING COMMANDS (Continued)

5. Only 10 significant digits may be used for the frequency command and 2½ significant digits for the amplitude command. An SRQ will be generated if the number of significant digits is exceeded.
6. The Display Modifier must first be activated with the M[ODIFY ON command before the other modify commands can be used.
7. The execute command causes the output of the synthesizer to change to the new values. Although the display changes on the transfer of data commands, the output will not change until the E[XECUTE command is sent.
8. The REV command gives the current software revision level — one ASCII character.
9. Command recall allows the user to read the last command over the GPIB. It is used when an SRQ is generated and the user wishes to determine where the error in the command occurred.
10. The state command gives the current frequency, amplitude, and rf output status (on/off) in one ASCII string.
11. The help command permits the user to read the allowable commands used for programming the 5155A into one 500 byte string array.
12. The symbol "@" is used to concatenate (or join) multiple commands and to provide compatibility between the 5155A and 5156A. For example:

    "FREQ 125M @ AMPL 13DB" — for 5155A
    "F125MA13" or "FREQ 125M AMPL 13DB" — for 5156A

APPENDIX C
MODEL 5156A GPIB (IEEE-488) PROGRAMMING COMMAND SUMMARY (Excluding GPIB Command Groups Given in Appendix A)

Control and Data Names	ASCII Primary Command	ASCII Secondary Command	ASCII Minimum Command
Frequency	F	—	F
Amplitude	A	—	A
Decimal Point	.	—	.
Numeric Data	0,1,2,...9	—	0,1,2,...9
Frequency Terminator	—	M[HZ	M
	—	K[HZ	K
	—	[HZ	—
Amplitude Terminator	—	[DB	—

NOTES TO PROGRAMMING COMMANDS

1. Only UPPER case (capital) letters may be used.
2. More readable statements may be used by adding additional letters as long as these letters do not include the reserved letters, F & A. For example:

   "F", "FREQ", "FRQ", "FREQ = ", and "FREQUENCY IS" are all acceptable

3. Amplitude level is programmed in steps of 0.1 dB from +3.1 dBm to +13.0 dBm and does not require a terminator (i.e., 12.4 dBm programs as "A12.4" or "A12.4DB")
4. Amplitude **cannot** be programmed in units of mV or volts.
5. The 5156A output is updated as soon as the carriage return (decimal 13), is received.
6. Multiple commands may be joined on one line as follows:

   WRITE @707: "F25MA10.3"
   WRITE @707: "F25M & A10.3"

MP MASTER
MA35680